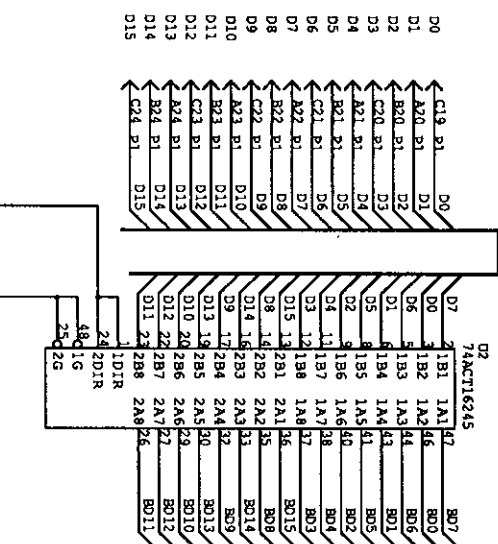
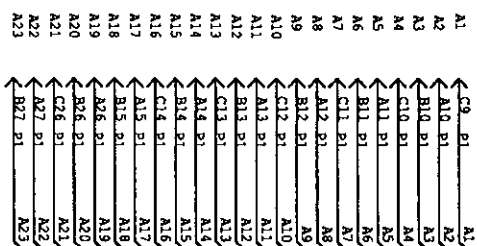
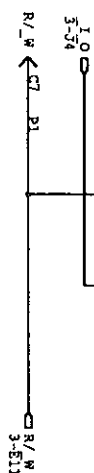


Portable Memory Revision History
Revision A 11/12/92 Original
Revision B 02/09/93 Update Sleep Cnt. to 22x10
convert AT750 to 22x10

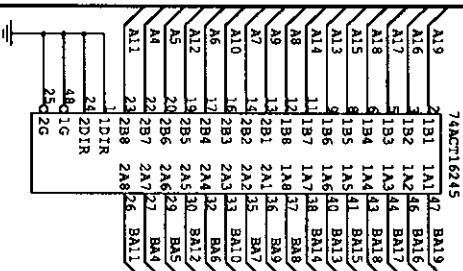
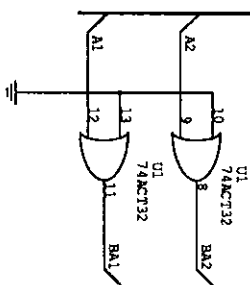
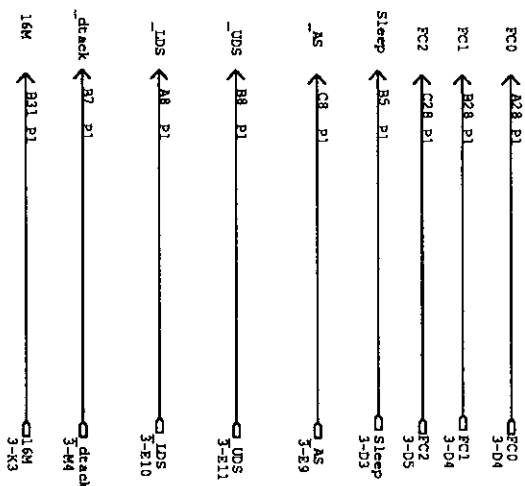


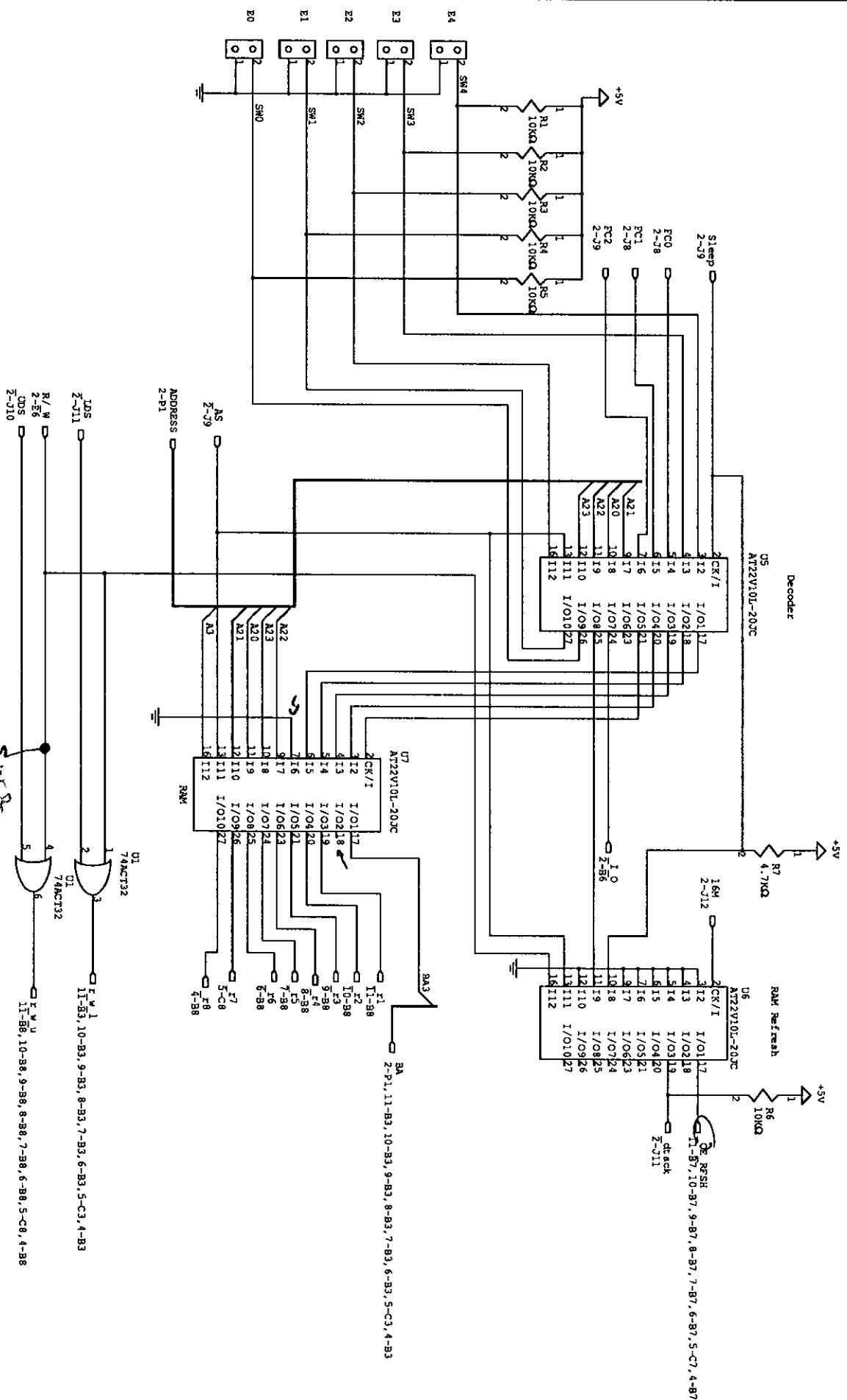
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11-C1,10-C1,9-C1,8-C1,7-C1,6-C1,5-D1,4-C1

ADDRESS
3-89



BA
3-17,11-B3,10-B3,9-B3,8-B3,7-B3,6-B3,5-C3,4-C3





BDATA 2-F1,11-C1,10-C1,9-C1,8-C1,7-C1,6-C1,5-D1

3-L10,11-B3,10-B3,9-B3,8-B3,7-B3,6-B3,5-C3
3-L7,2-P1,11-B3,10-B3,9-B3,8-B3,7-B3,6-B3,5-C3

3-M3,11-B7,10-B7,9-B7,8-B7,7-B7,6-B7,5-C7

3-L11,11-B8,10-B8,9-B8,8-B8,7-B8,6-B8,5-C8

C81			U80		
658512			558512		
BA1	12	A0	BA1	12	A0
BA2	11	A1	BA2	11	A1
BA3	10	A2	BA3	10	A2
BA4	9	A3	BA4	9	A3
BA5	8	A4	BA5	8	A4
BA6	7	A5	BA6	7	A5
BA7	6	A6	BA7	6	A6
BA8	5	A7	BA8	5	A7
BA9	4	A8	BA9	4	A8
BA10	3	A9	BA10	3	A9
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BA13	12	A12	BA13	12	A12
BA14	11	A13	BA14	11	A13
BA15	10	A14	BA15	10	A14
BA16	9	A15	BA16	9	A15
BA17	8	A16	BA17	8	A16
BA18	7	A17	BA18	7	A17
BA19	6	A18	BA19	6	A18
I/O0 13 BD0			I/O0 13 BD0		
I/O1 14 BD1			I/O1 14 BD1		
I/O2 15 BD2			I/O2 15 BD2		
I/O3 16 BD3			I/O3 16 BD3		
I/O4 17 BD4			I/O4 17 BD4		
I/O5 18 BD5			I/O5 18 BD5		
I/O6 19 BD6			I/O6 19 BD6		
I/O7 20 BD7			I/O7 20 BD7		
I/O8 21 BD8			I/O8 21 BD8		
I/O9 22 BD9			I/O9 22 BD9		
I/O10 23 BD10			I/O10 23 BD10		
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I/O12 25 BD12			I/O12 25 BD12		
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I/O21 34 BD21			I/O21 34 BD21		
I/O22 35 BD22			I/O22 35 BD22		
I/O23 36 BD23			I/O23 36 BD23		
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I/O32 45 BD32			I/O32 45 BD32		
I/O33 46 BD33			I/O33 46 BD33		
I/O34 47 BD34			I/O34 47 BD34		
I/O35 48 BD35			I/O35 48 BD35		
I/O36 49 BD36			I/O36 49 BD36		
I/O37 50 BD37			I/O37 50 BD37		
I/O38 51 BD38			I/O38 51 BD38		
I/O39 52 BD39			I/O39 52 BD39		
I/O40 53 BD40			I/O40 53 BD40		
I/O41 54 BD41			I/O41 54 BD41		
I/O42 55 BD42			I/O42 55 BD42		
I/O43 56 BD43			I/O43 56 BD43		
I/O44 57 BD44			I/O44 57 BD44		
I/O45 58 BD45			I/O45 58 BD45		
I/O46 59 BD46			I/O46 59 BD46		
I/O47 60 BD47			I/O47 60 BD47		
I/O48 61 BD48			I/O48 61 BD48		
I/O49 62 BD49			I/O49 62 BD49		
I/O50 63 BD50			I/O50 63 BD50		
I/O51 64 BD51			I/O51 64 BD51		
I/O52 65 BD52			I/O52 65 BD52		
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I/O54 67 BD54			I/O54 67 BD54		
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I/O56 69 BD56			I/O56 69 BD56		
I/O57 70 BD57			I/O57 70 BD57		
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I/O60 73 BD60			I/O60 73 BD60		
I/O61 74 BD61			I/O61 74 BD61		
I/O62 75 BD62			I/O62 75 BD62		
I/O63 76 BD63			I/O63 76 BD63		
I/O64 77 BD64			I/O64 77 BD64		
I/O65 78 BD65			I/O65 78 BD65		
I/O66 79 BD66			I/O66 79 BD66		
I/O67 80 BD67			I/O67 80 BD67		
I/O68 81 BD68			I/O68 81 BD68		
I/O69 82 BD69			I/O69 82 BD69		
I/O70 83 BD70			I/O70 83 BD70		
I/O71 84 BD71			I/O71 84 BD71		
I/O72 85 BD72			I/O72 85 BD72		
I/O73 86 BD73			I/O73 86 BD73		
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I/O75 88 BD75			I/O75 88 BD75		
I/O76 89 BD76			I/O76 89 BD76		
I/O77 90 BD77			I/O77 90 BD77		
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I/O79 92 BD79			I/O79 92 BD79		
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I/O81 94 BD81			I/O81 94 BD81		
I/O82 95 BD82			I/O82 95 BD82		
I/O83 96 BD83			I/O83 96 BD83		
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I/O99 112 BD99			I/O99 112 BD99		
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3-17,2-F1,11-B3,10-B3,9-B3,8-B3,7-B3,6-B3,4-B3

3-111,11-B8,10-B8,9-B8,8-B8,7-B8,6-B8,4-B8

3-111,11-B8,10-B8,9-B8,8-B8,7-B8,6-B8,4-B8

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BA5	8	A4	
BA6	7	A5	
BA7	6	A6	
BA8	5	A7	
BA9	4	A8	
BA10	3	A9	
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BA294	7	A5	
BA295	6	A6	
BA296	5	A7	
BA297	4	A8	
BA298	3	A9	
BA299	2	A10	
BA300	1	A11	

BDATA 2-P1,11-C1,10-C1,9-C1,8-C1,7-C1,5-D1,4-C1

3-L10,11-B3,10-B3,9-B3,8-B3,7-B3,5-C3,4-B3

3-L7,2-P1,11-B3,10-B3,9-B3,8-B3,7-B3,5-C3,4-B3

OE REFRESH 3-M1,11-B7,10-B7,9-B7,8-B7,7-B7,5-C7,4-B7

3-L8

3-L11,11-B8,10-B8,9-B8,8-B8,7-B8,5-C8,4-B8

U61
658512

24 OE/REFSH

22 CE

29 WE

BA1	12	A0	1/00	13	BD0
BA2	11	A1	1/01	14	BD1
BA3	10	A2	1/02	15	BD2
BA4	9	A3	1/03	16	BD3
BA5	8	A4	1/04	17	BD4
BA6	7	A5	1/05	18	BD5
BA7	6	A6	1/06	19	BD6
BA8	5	A7	1/07	20	BD7
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	28	A13			
BA15	27	A14			
BA16	26	A15			
BA17	25	A16			
BA18	24	A17			
BA19	23	A18			

U60
658512

24 OE/REFSH

22 CE

29 WE

BA1	12	A0	1/00	13	BD8
BA2	11	A1	1/01	14	BD9
BA3	10	A2	1/02	15	BD10
BA4	9	A3	1/03	16	BD11
BA5	8	A4	1/04	17	BD12
BA6	7	A5	1/05	18	BD13
BA7	6	A6	1/06	19	BD14
BA8	5	A7	1/07	20	BD15
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	28	A13			
BA15	27	A14			
BA16	26	A15			
BA17	25	A16			
BA18	24	A17			
BA19	23	A18			

DATA 0
2-F1,11-C1,10-C1,9-C1,8-C1,6-C1,5-D1,4-C1

US1
658512

3-W1 0
3-L10,11-B3,10-B3,9-B3,8-B3,6-B3,5-C3,4-B3
BA 0
3-L7,2-P1,11-B3,10-B3,9-B3,8-B3,6-B3,5-C3,4-B3

BA1	12	A0	I/O0 13	BD0
BA2	11	A1	I/O1 14	BD1
BA3	10	A2	I/O2 15	BD2
BA4	9	A3	I/O3 17	BD3
BA5	8	A4	I/O4 18	BD4
BA6	7	A5	I/O5 19	BD5
BA7	6	A6	I/O6 20	BD6
BA8	5	A7	I/O7 21	BD7
BA9	4	A8		
BA10	3	A9		
BA11	2	A10		
BA12	1	A11		
BA13	0	A12		
BA14	28	A13		
BA15	27	A14		
BA16	26	A15		
BA17	25	A16		
BA18	24	A17		
BA19	23	A18		

OE/RESH 0
3-W3,11-B7,10-B7,9-B7,8-B7,6-B7,5-C7,4-B7

US0
658512

3-W0 0
3-L8 0
3-L1,11-B8,10-B8,9-B8,8-B8,6-B8,5-C8,4-B8

BA1	12	A0	I/O0 13	BD8
BA2	11	A1	I/O1 14	BD9
BA3	10	A2	I/O2 15	BD10
BA4	9	A3	I/O3 17	BD11
BA5	8	A4	I/O4 18	BD12
BA6	7	A5	I/O5 19	BD13
BA7	6	A6	I/O6 20	BD14
BA8	5	A7	I/O7 21	BD15
BA9	4	A8		
BA10	3	A9		
BA11	2	A10		
BA12	1	A11		
BA13	0	A12		
BA14	28	A13		
BA15	27	A14		
BA16	26	A15		
BA17	25	A16		
BA18	24	A17		
BA19	23	A18		

BDATA 2-F1,11-C1,10-C1,9-C1,7-C1,6-C1,5-D1,4-C1

U41
658512

3-M1 3-M10,11-B3,10-B3,9-B3,7-B3,6-B3,5-C3,4-B3

3-L7,2-F1,11-B3,10-B3,9-B3,7-B3,6-B3,5-C3,4-B3

BA1	12	A0	I/O0	13	BD0
BA2	11	A1	I/O1	14	BD1
BA3	10	A2	I/O2	15	BD2
BA4	9	A3	I/O3	16	BD3
BA5	8	A4	I/O4	17	BD4
BA6	7	A5	I/O5	18	BD5
BA7	6	A6	I/O6	19	BD6
BA8	5	A7	I/O7	20	BD7
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	28	A12			
BA14	27	A13			
BA15	26	A14			
BA16	25	A15			
BA17	24	A16			
BA18	23	A17			
BA19	22	A18			

OE/RESH 3-W3,11-B7,10-B7,9-B7,7-B7,6-B7,5-C7,4-B7

3-L8 3-L8 24 OE/RESH 22 CE 29 WE

3-VU 3-VU 3-L11,11-B8,10-B8,9-B8,7-B8,6-B8,5-C8,4-B8

BA1	12	A0	I/O0	13	BD8
BA2	11	A1	I/O1	14	BD9
BA3	10	A2	I/O2	15	BD10
BA4	9	A3	I/O3	16	BD11
BA5	8	A4	I/O4	17	BD12
BA6	7	A5	I/O5	18	BD13
BA7	6	A6	I/O6	19	BD14
BA8	5	A7	I/O7	20	BD15
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	28	A12			
BA14	27	A13			
BA15	26	A14			
BA16	25	A15			
BA17	24	A16			
BA18	23	A17			
BA19	22	A18			

BDATA 2-FL,11-C1,10-C1,8-C1,7-C1,6-C1,5-D1,4-C1

3-FL,11-B3,10-B3,8-B3,7-B3,6-B3,5-C3,4-B3

3-L7,2-P1,11-B3,10-B3,8-B3,7-B3,6-B3,5-C3,4-B3

U31
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24 OE/REFSH

22 CE

29 WE

BA1	12	A0	I/O0	13	BD0
BA2	11	A1	I/O1	14	BD1
BA3	10	A2	I/O2	15	BD2
BA4	9	A3	I/O3	16	BD3
BA5	8	A4	I/O4	17	BD4
BA6	7	A5	I/O5	18	BD5
BA7	6	A6	I/O6	19	BD6
BA8	5	A7	I/O7	20	BD7
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	28	A13			
BA15	27	A14			
BA16	26	A15			
BA17	25	A16			
BA18	24	A17			
BA19	23	A18			

U30
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24 OE/REFSH

22 CE

29 WE

BA1	12	A0	I/O0	13	BD8
BA2	11	A1	I/O1	14	BD9
BA3	10	A2	I/O2	15	BD10
BA4	9	A3	I/O3	16	BD11
BA5	8	A4	I/O4	17	BD12
BA6	7	A5	I/O5	18	BD13
BA7	6	A6	I/O6	19	BD14
BA8	5	A7	I/O7	20	BD15
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	28	A13			
BA15	27	A14			
BA16	26	A15			
BA17	25	A16			
BA18	24	A17			
BA19	23	A18			

DATA 1
2-F1,11-C1,9-C1,8-C1,7-C1,6-C1,5-D1,4-C1

3-L10, 11-B3, 9-B3, 8-B3, 7-B3, 6-B3, 5-C3, 4-B3

3-L7, 2-P1, 11-B3, 9-B3, 8-B3, 7-B3, 6-B3, 5-C3, 4-B3

U21
658512

24 COE/REFSH

22 CE

29 WE

BA1

BA2

BA3

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BA336

BA337

BDATA 2-E1,10-C1,9-C1,8-C1,7-C1,6-C1,5-D1,4-C1

U11
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3-L10,10-B3,9-B3,8-B3,7-B3,6-B3,5-C3,4-B3

BA 3-L7,2-E1,10-B3,9-B3,8-B3,7-B3,6-B3,5-C3,4-B3

BA1	12	A0	I/O0	13	BD0
BA2	11	A1	I/O1	14	BD1
BA3	10	A2	I/O2	15	BD2
BA4	9	A3	I/O3	16	BD3
BA5	8	A4	I/O4	17	BD4
BA6	7	A5	I/O5	18	BD5
BA7	6	A6	I/O6	19	BD6
BA8	5	A7	I/O7	20	BD7
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	28	A13			
BA15	27	A14			
BA16	26	A15			
BA17	25	A16			
BA18	24	A17			
BA19	23	A18			

08-RFSH 3-W3,10-B7,9-B7,8-B7,7-B7,6-B7,5-C7,4-B7

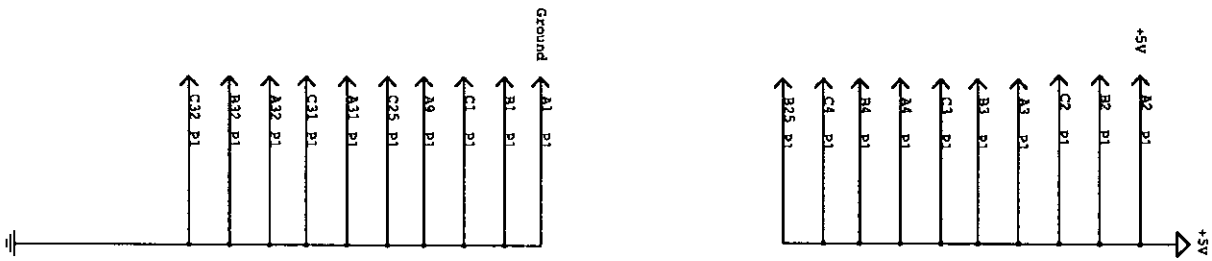
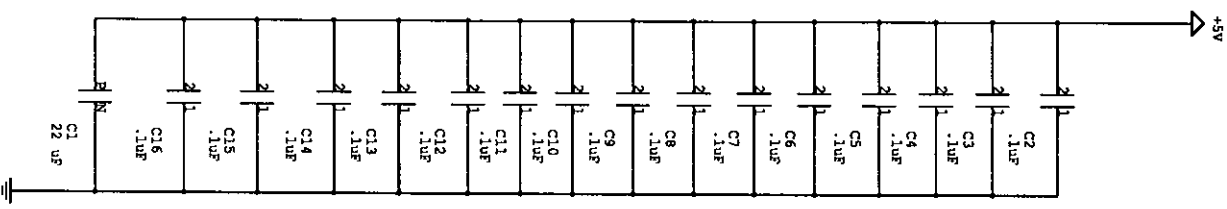
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3-L11,10-B8,9-B8,8-B8,7-B8,6-B8,5-C8,4-B8

BA1	12	A0	I/O0	13	BD8
BA2	11	A1	I/O1	14	BD9
BA3	10	A2	I/O2	15	BD10
BA4	9	A3	I/O3	16	BD11
BA5	8	A4	I/O4	17	BD12
BA6	7	A5	I/O5	18	BD13
BA7	6	A6	I/O6	19	BD14
BA8	5	A7	I/O7	20	BD15
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	28	A13			
BA15	27	A14			
BA16	26	A15			
BA17	25	A16			
BA18	24	A17			
BA19	23	A18			

Unless otherwise indicated
all caps: .1uF, 25V, 20%

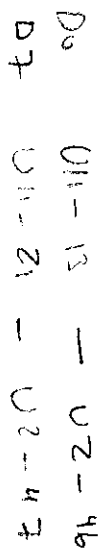
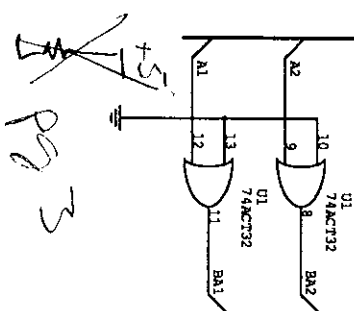
SPARE GATES

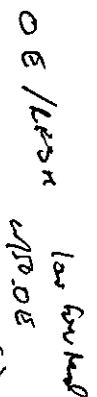


Reversible Memory REVISION HISTORY
REVISION A 11/12/92 Original



Keith Leisner/Designer
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PAGE 1 OF 11
Power
REV A 11/12/92





3-T¹0, 11-B3, 10-B3, 9-B3, 8-B3, 7-B3, 6-B3, 5-C3
11-B3, 10-B3, 9-B3, 8-B3, 7-B3, 6-B3, 5-C3, 2-P1

240 OE/REFSH

[illegible]

24 **DOE/RE SH**

OE RESH $\square$ 3-85, 1.1-B7, 1.0-87, 9-B7, 8-B7, 7-B7, 6-B7, 5-C7
 Zr^{8+} $\square$ 3-19
 Zr^{4+} $\square$ 3-17, 1.1-B8, 1.0-88, 9-B8, 8-B8, 7-B8, 6-B8, 5-C8

B01	12	A0
B02	11	A1
B03	10	A2
B04	9	A3
B05	8	A4
B06	7	A5
B07	6	A6
B08	5	A7
B09	27	A8
B10	26	A9
B11	25	A10
B12	25	A11
B13	4	A12
B14	28	A13
B15	3	A14
B16	31	A15
B17	2	A16
B18	30	A17
B19	1	A18

P1222 game
 P1224 all
 P1229 pass →
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 its even pass
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over
under

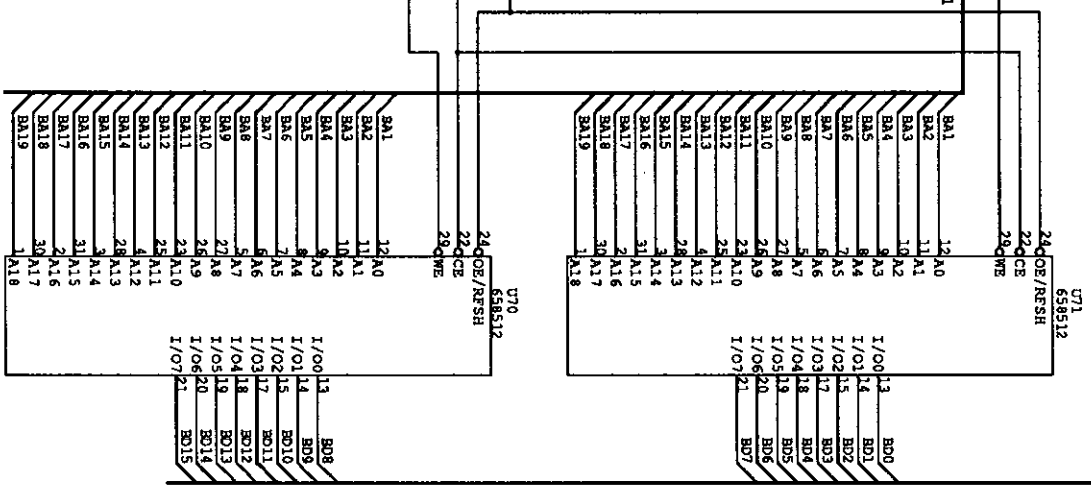
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BDATA 11-C1,10-C1,9-C1,8-C1,7-C1,6-C1,4-C1,2-F1

3-10,11-B3,10-B3,9-B3,8-B3,7-B3,6-B3,4-B3
BA 11-B3,10-B3,9-B3,8-B3,7-B3,6-B3,4-B3,2-F1

OE REFRESH 3-15,11-B7,10-B7,9-B7,8-B7,7-B7,6-B7,4-B7

3-17,11-B8,10-B8,9-B8,8-B8,7-B8,6-B8,4-B8



DATA 11-C1,10-C1,9-C1,8-C1,7-C1,5-D1,4-C1,2-F1

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3-10,11-B3,10-B3,9-B3,8-B3,7-B3,5-C3,4-B3

11-B3,10-B3,9-B3,8-B3,7-B3,5-C3,4-B3,2-P1

BA1	12	A0	I/O0	13	BD0
BA2	11	A1	I/O1	14	BD1
BA3	10	A2	I/O2	15	BD2
BA4	9	A3	I/O3	16	BD3
BA5	8	A4	I/O4	17	BD4
BA6	7	A5	I/O5	18	BD5
BA7	6	A6	I/O6	19	BD6
BA8	5	A7	I/O7	20	BD7
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	0	A13			
BA15	0	A14			
BA16	0	A15			
BA17	0	A16			
BA18	0	A17			
BA19	0	A18			

D60
658512

3-45,11-B7,10-B7,9-B7,8-B7,7-B7,5-C7,4-B7

3-18

3-17,11-B8,10-B8,9-B8,8-B8,7-B8,5-C8,4-B8

BA1	12	A0	I/O0	13	BD0
BA2	11	A1	I/O1	14	BD9
BA3	10	A2	I/O2	15	BD10
BA4	9	A3	I/O3	16	BD11
BA5	8	A4	I/O4	17	BD12
BA6	7	A5	I/O5	18	BD13
BA7	6	A6	I/O6	19	BD14
BA8	5	A7	I/O7	20	BD15
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	0	A13			
BA15	0	A14			
BA16	0	A15			
BA17	0	A16			
BA18	0	A17			
BA19	0	A18			

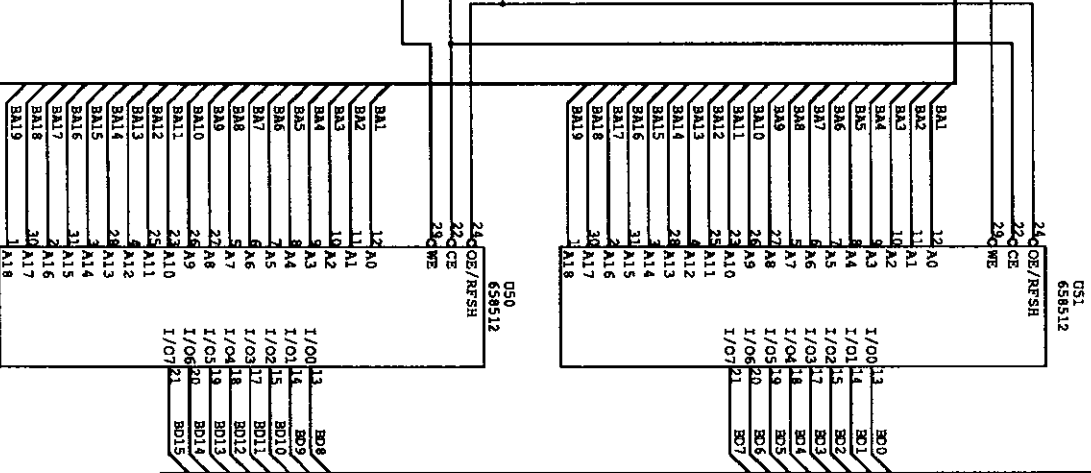
Susan Martin Xi lix
408 879 4917
Lisc. 390
408 559 9327
N 581 9600

BDATA 10-C1,10-C1,9-C1,8-C1,6-C1,5-D1,4-C1,2-F1

3-10,11-B3,10-B3,9-B3,8-B3,6-B3,5-C3,4-B3
BA 11-B3,10-B3,9-B3,8-B3,6-B3,5-C3,4-B3,2-P1

OE REFRESH 3-10,11-B7,10-B7,9-B7,8-B7,6-B7,5-C7,4-B7

3-10,11-B8,10-B8,9-B8,8-B8,6-B8,5-C8,4-B8



BDATA 11-C1,10-C1,9-C1,7-C1,6-C1,5-D1,4-C1,2-F1

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3-10,11-B3,10-B3,9-B3,7-B3,6-B3,5-C3,4-B3

11-B3,10-B3,9-B3,7-B3,6-B3,5-C3,4-B3,2-P1

BA1	12	A0	I/O0	13	BD0
BA2	11	A1	I/O1	14	BD1
BA3	10	A2	I/O2	15	BD2
BA4	9	A3	I/O3	16	BD3
BA5	8	A4	I/O4	17	BD4
BA6	7	A5	I/O5	18	BD5
BA7	6	A6	I/O6	19	BD6
BA8	5	A7	I/O7	20	BD7
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	28	A13			
BA15	31	A14			
BA16	30	A15			
BA17	29	A16			
BA18	27	A17			
BA19	26	A18			

OE RESH 3-10,11-B7,10-B7,9-B7,7-B7,6-B7,5-C7,4-B7

3-10,11-B7,10-B7,9-B7,7-B7,6-B7,5-C7,4-B7

BA1	12	A0	I/O0	13	BD8
BA2	11	A1	I/O1	14	BD9
BA3	10	A2	I/O2	15	BD10
BA4	9	A3	I/O3	16	BD11
BA5	8	A4	I/O4	17	BD12
BA6	7	A5	I/O5	18	BD13
BA7	6	A6	I/O6	19	BD14
BA8	5	A7	I/O7	20	BD15
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	28	A13			
BA15	31	A14			
BA16	30	A15			
BA17	29	A16			
BA18	27	A17			
BA19	26	A18			

3-10,11-B8,10-B8,9-B8,7-B8,6-B8,5-C8,4-B8

BDXNA
11-C1,10-C1,8-C1,7-C1,5-C1,4-C1,2-F1

U31
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3-10,11-B3,10-B3,8-B3,7-B3,6-B3,5-C3,4-B3

11-B3,10-B3,8-B3,7-B3,6-B3,5-C3,4-B3,2-F1

BA1	12	A0	I/O0	13	BD0
BA2	11	A1	I/O1	14	BD1
BA3	10	A2	I/O2	15	BD2
BA4	9	A3	I/O3	16	BD3
BA5	8	A4	I/O4	17	BD4
BA6	7	A5	I/O5	18	BD5
BA7	6	A6	I/O6	19	BD6
BA8	5	A7	I/O7	20	BD7
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	28	A13			
BA15	27	A14			
BA16	26	A15			
BA17	25	A16			
BA18	24	A17			
BA19	23	A18			

OE/RESH
3-10,11-B7,10-B7,8-B7,7-B7,6-B7,5-C7,4-B7

3-10,11-B7,10-B7,8-B7,7-B7,6-B7,5-C7,4-B7

BA1	12	A0	I/O0	13	BD8
BA2	11	A1	I/O1	14	BD9
BA3	10	A2	I/O2	15	BD10
BA4	9	A3	I/O3	16	BD11
BA5	8	A4	I/O4	17	BD12
BA6	7	A5	I/O5	18	BD13
BA7	6	A6	I/O6	19	BD14
BA8	5	A7	I/O7	20	BD15
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	28	A13			
BA15	27	A14			
BA16	26	A15			
BA17	25	A16			
BA18	24	A17			
BA19	23	A18			

BDATA 11-C1,9-C1,8-C1,7-C1,6-C1,5-D1,4-C1,2-F1

3-10,11-B3,9-B3,8-B3,7-B3,6-B3,5-C3,4-B3

11-B3,9-B3,8-B3,7-B3,6-B3,5-C3,4-B3,2-F1

U21
658512

24 OE/REFSH

22 CE

29 WE

BA1	12	A0	I/O0	13	BD0
BA2	11	A1	I/O1	14	BD1
BA3	10	A2	I/O2	15	BD2
BA4	9	A3	I/O3	16	BD3
BA5	8	A4	I/O4	17	BD4
BA6	7	A5	I/O5	18	BD5
BA7	6	A6	I/O6	19	BD6
BA8	5	A7	I/O7	20	BD7
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	31	A13			
BA15	30	A14			
BA16	29	A15			
BA17	28	A16			
BA18	27	A17			
BA19	26	A18			

OE/REFSH 3-10,11-B7,9-B7,8-B7,7-B7,6-B7,5-C7,4-B7

3-17

U20
658512

24 OE/REFSH

22 CE

29 WE

BA1	12	A0	I/O0	13	BD0
BA2	11	A1	I/O1	14	BD1
BA3	10	A2	I/O2	15	BD2
BA4	9	A3	I/O3	16	BD3
BA5	8	A4	I/O4	17	BD4
BA6	7	A5	I/O5	18	BD5
BA7	6	A6	I/O6	19	BD6
BA8	5	A7	I/O7	20	BD7
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	31	A13			
BA15	30	A14			
BA16	29	A15			
BA17	28	A16			
BA18	27	A17			
BA19	26	A18			

BDXNA 10-C1,9-C1,8-C1,7-C1,6-C1,5-D1,4-C1,2-F1

011
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5-T10,10-B3,9-B3,8-B3,7-B3,6-B3,5-C3,4-B3

BA 10-B3,9-B3,8-B3,7-B3,6-B3,5-C3,4-B3,2-P1

BA1	12	A0	I/O0	13	BD0
BA2	11	A1	I/O1	14	BD1
BA3	10	A2	I/O2	15	BD2
BA4	9	A3	I/O3	16	BD3
BA5	8	A4	I/O4	17	BD4
BA6	7	A5	I/O5	18	BD5
BA7	6	A6	I/O6	19	BD6
BA8	5	A7	I/O7	20	BD7
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	28	A13			
BA15	27	A14			
BA16	26	A15			
BA17	25	A16			
BA18	24	A17			
BA19	23	A18			

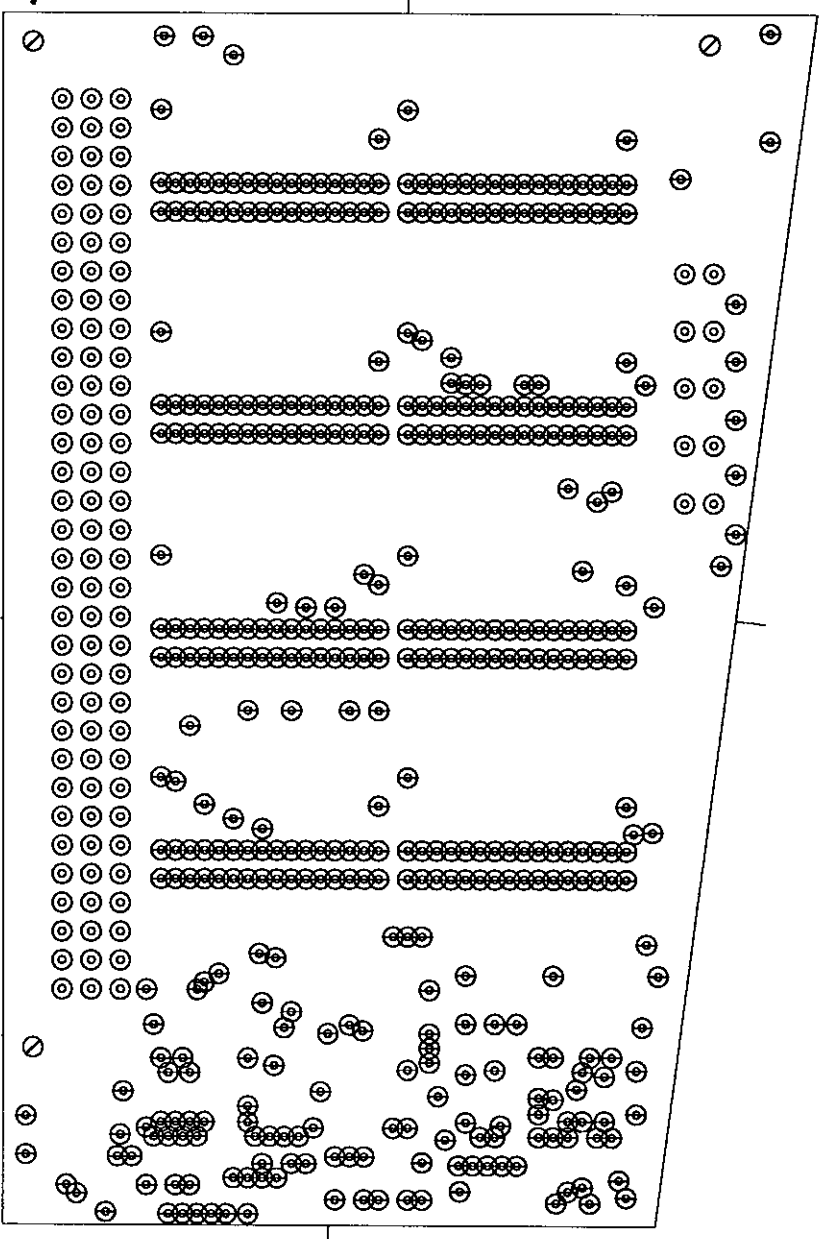
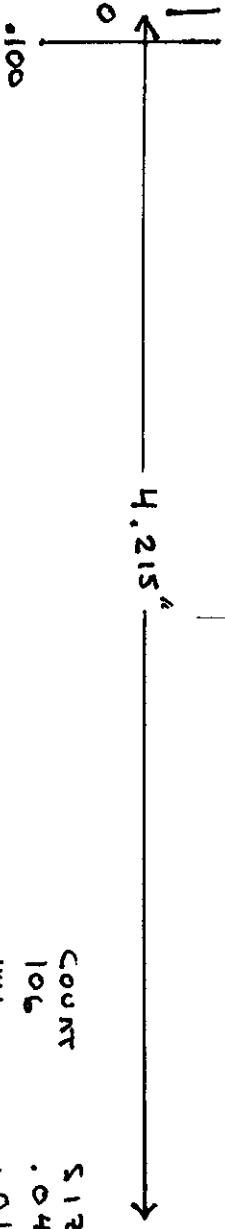
OE RSH 3-M5,10-B7,9-B7,8-B7,7-B7,6-B7,5-C7,4-B7

F1 3-T7,10-B8,9-B8,8-B8,7-B8,6-B8,5-C8,4-B8

BA1	12	A0	I/O0	13	BD8
BA2	11	A1	I/O1	14	BD9
BA3	10	A2	I/O2	15	BD10
BA4	9	A3	I/O3	16	BD11
BA5	8	A4	I/O4	17	BD12
BA6	7	A5	I/O5	18	BD13
BA7	6	A6	I/O6	19	BD14
BA8	5	A7	I/O7	20	BD15
BA9	4	A8			
BA10	3	A9			
BA11	2	A10			
BA12	1	A11			
BA13	0	A12			
BA14	28	A13			
BA15	27	A14			
BA16	26	A15			
BA17	25	A16			
BA18	24	A17			
BA19	23	A18			

7 7 0

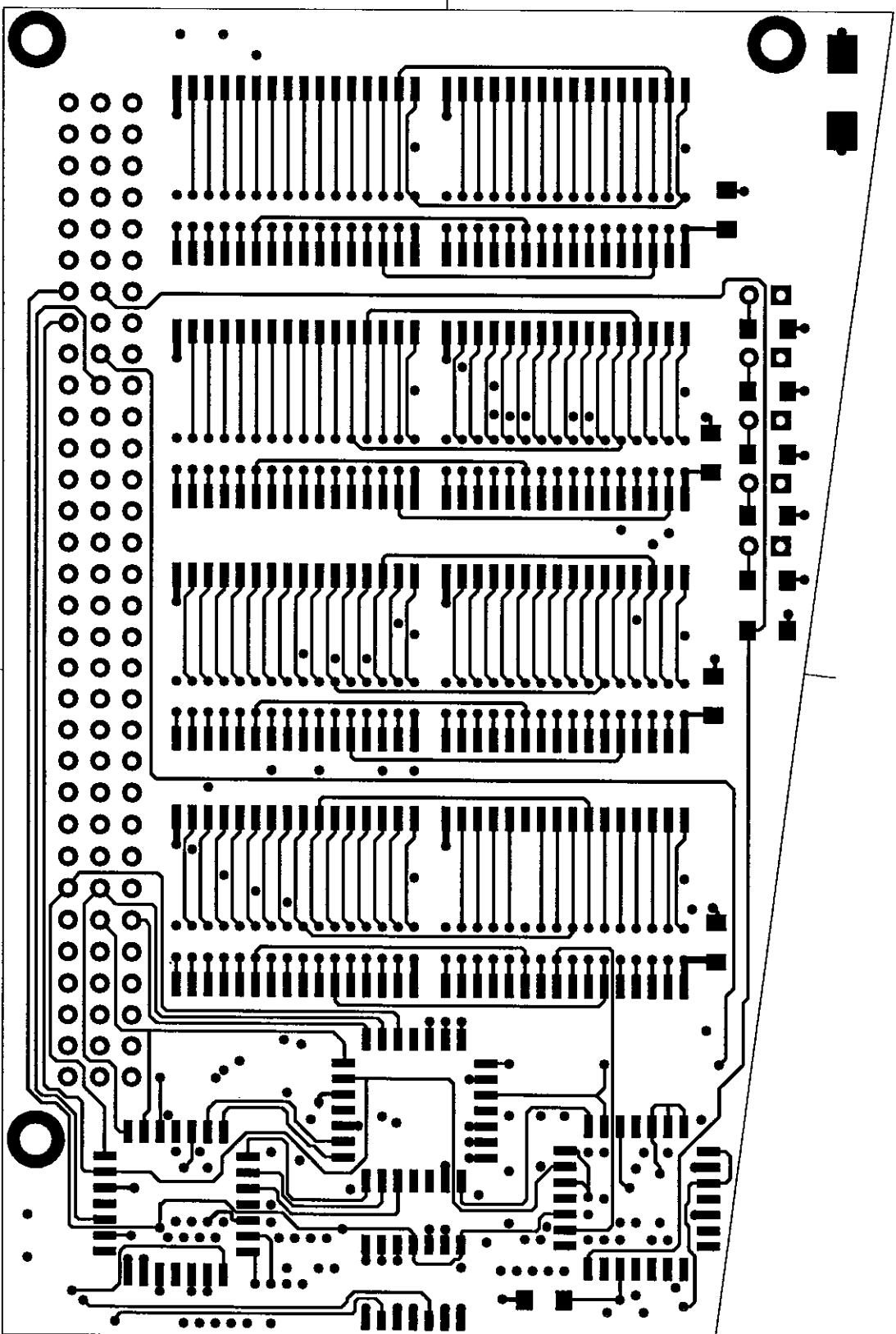
Jim 415-969-6385



Count	Size
106	.040
441	.013
3	.110

MacPort_R.01
Thu, Nov 12, 1992 8:24 PM
Hole Symbols Scale150%

.035	○	.038	⊖	.052	⊕	.002	⊗	.040	⊙
.040	⊖	.110	⊗			.005	⊗	.013	⊕
.125	⊗	.140	⊗	.004	⊕	.007	⊗	.006	⊗

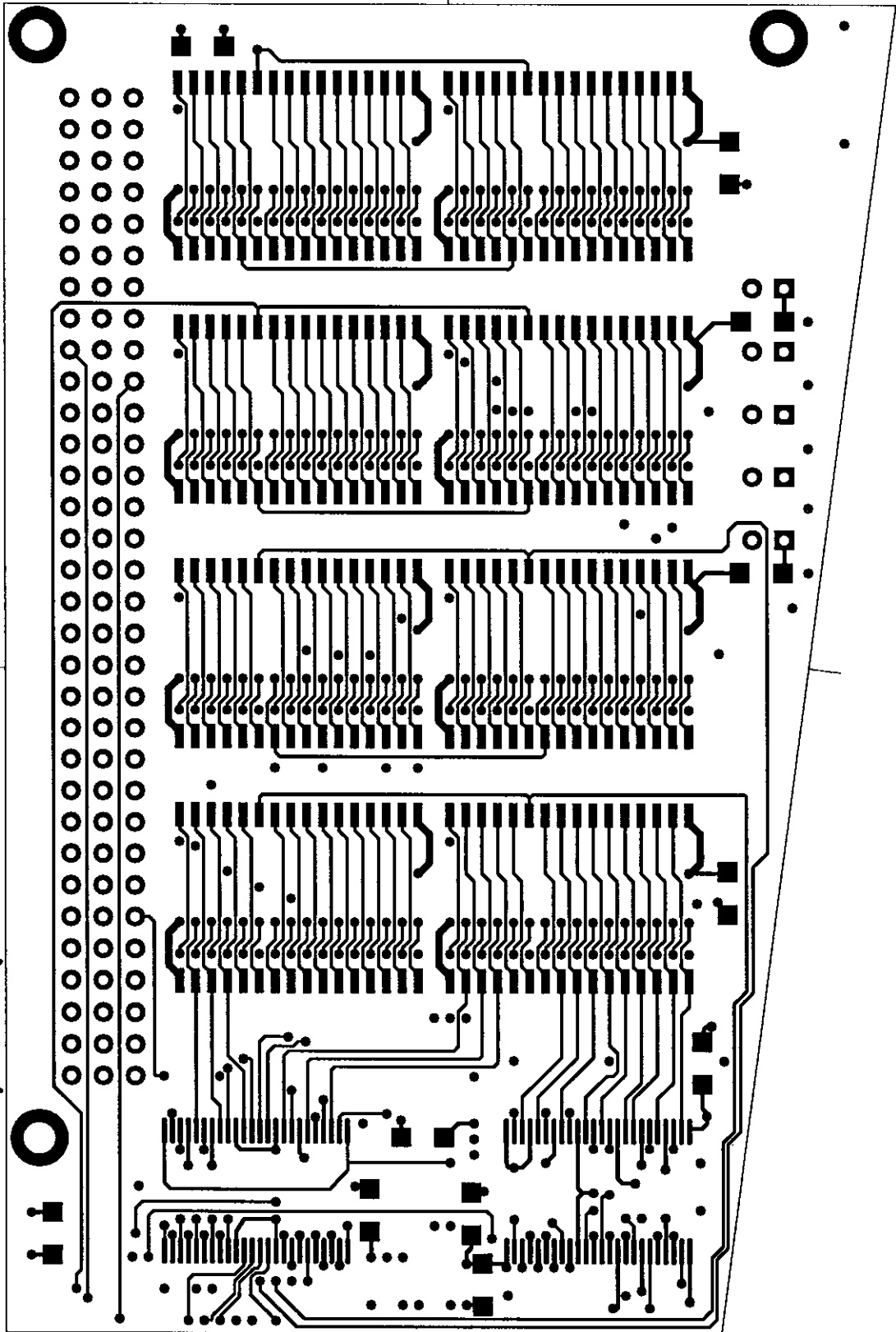


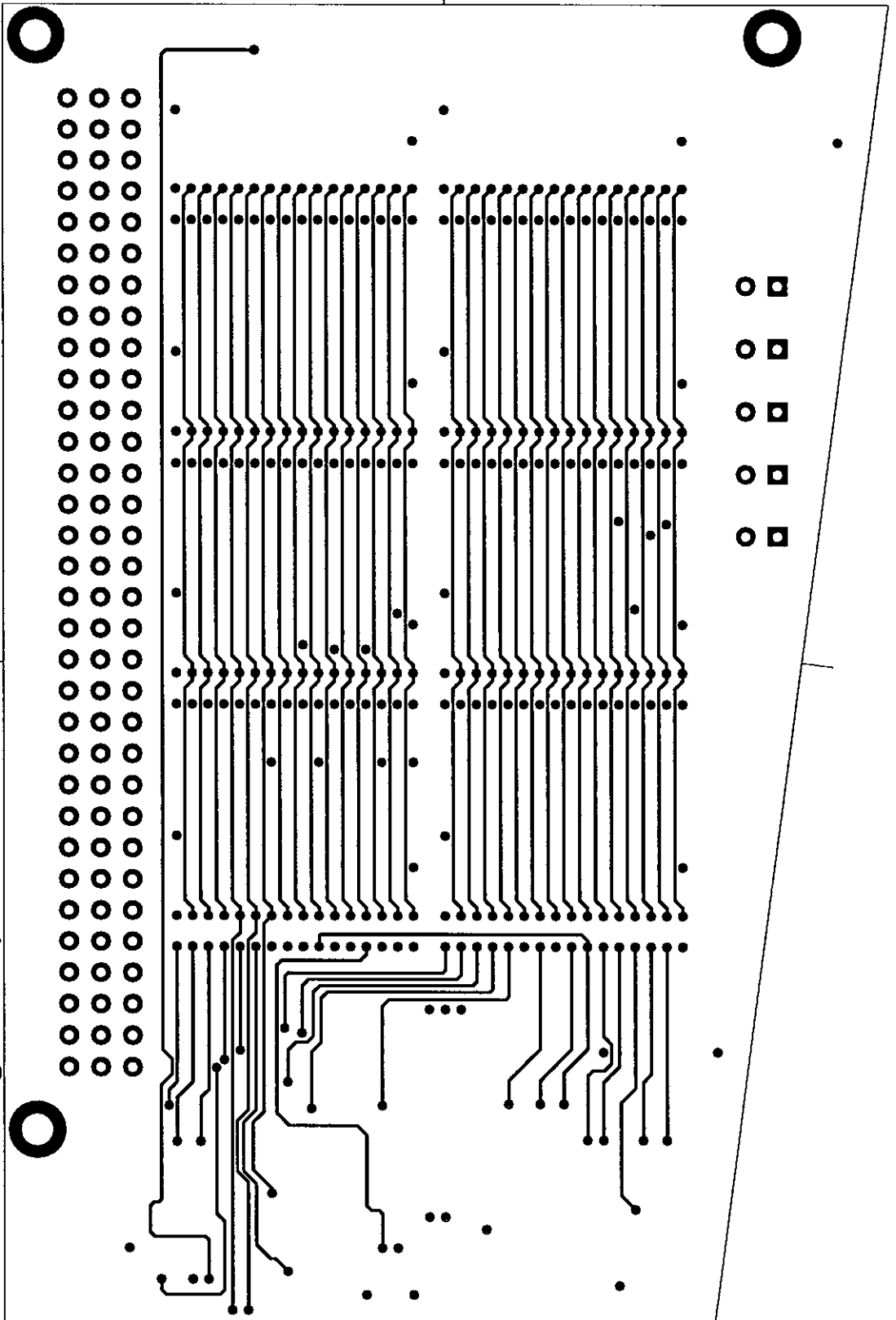
Layer 0

Board layer 1

ΕΚΚΕΚΟΛΗΝΑ Θ

Γράφει Γ



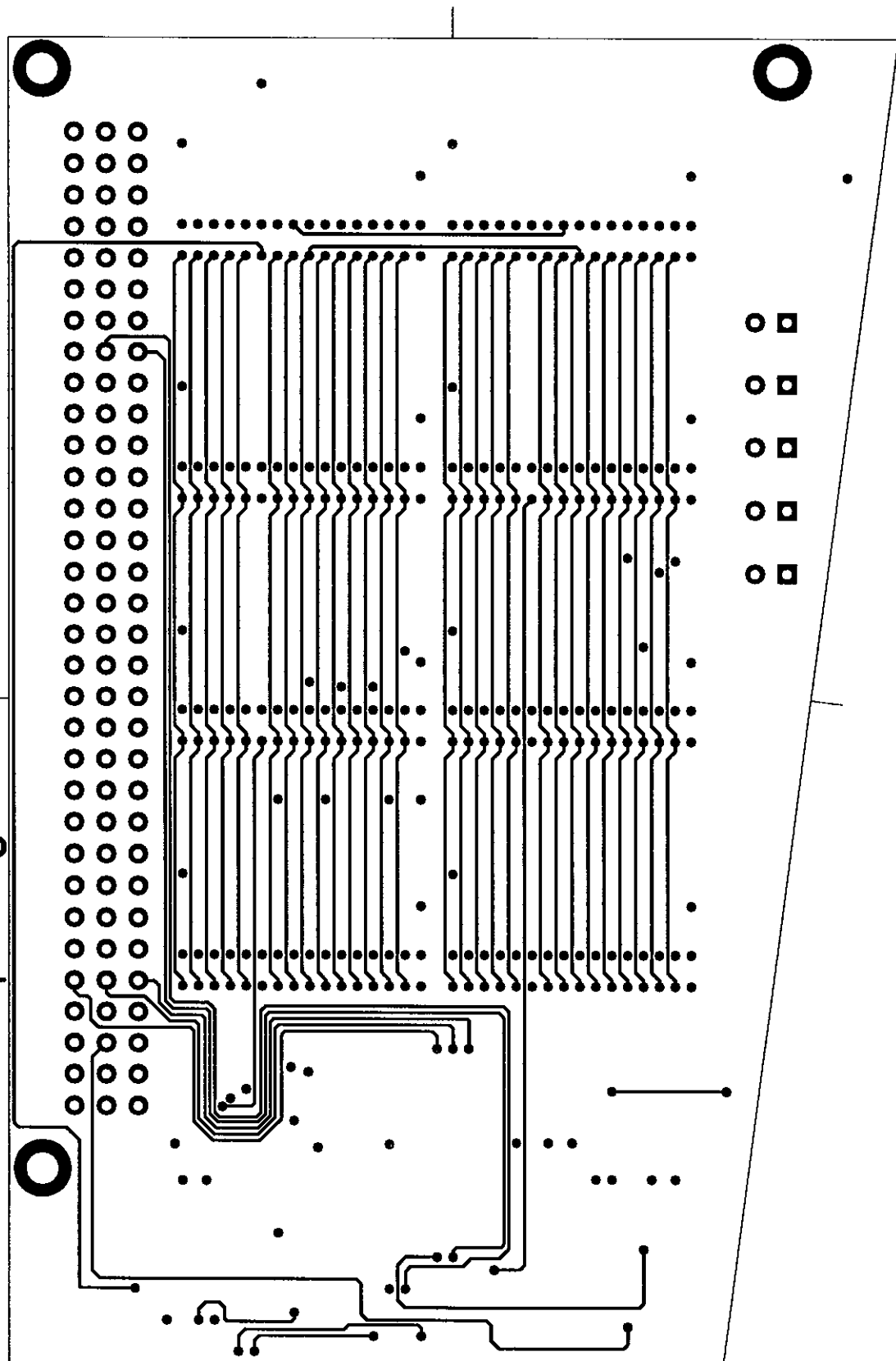


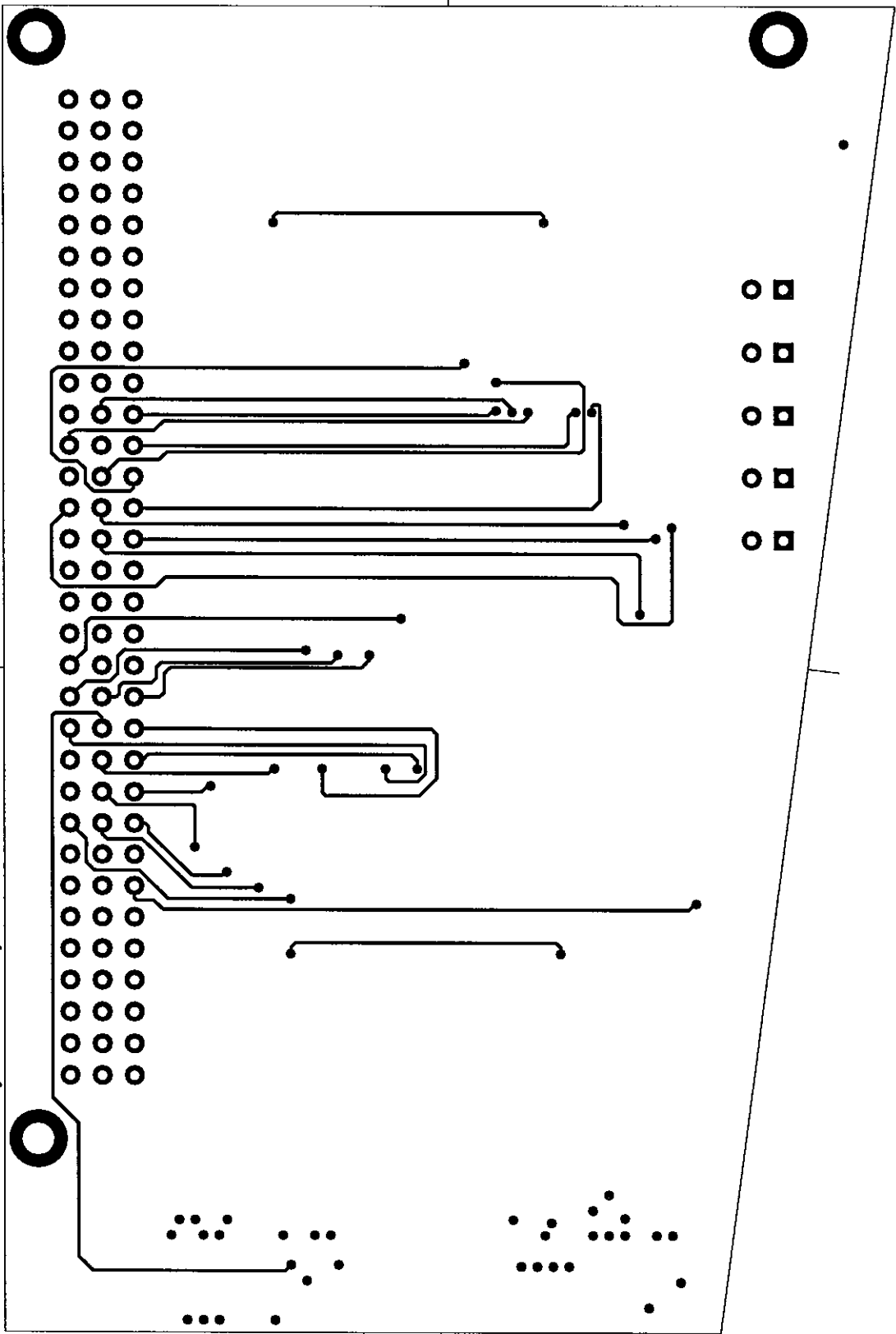
Layer 2

BOARD LAYER 2

ΕΚΔΟΣ 18/4/06

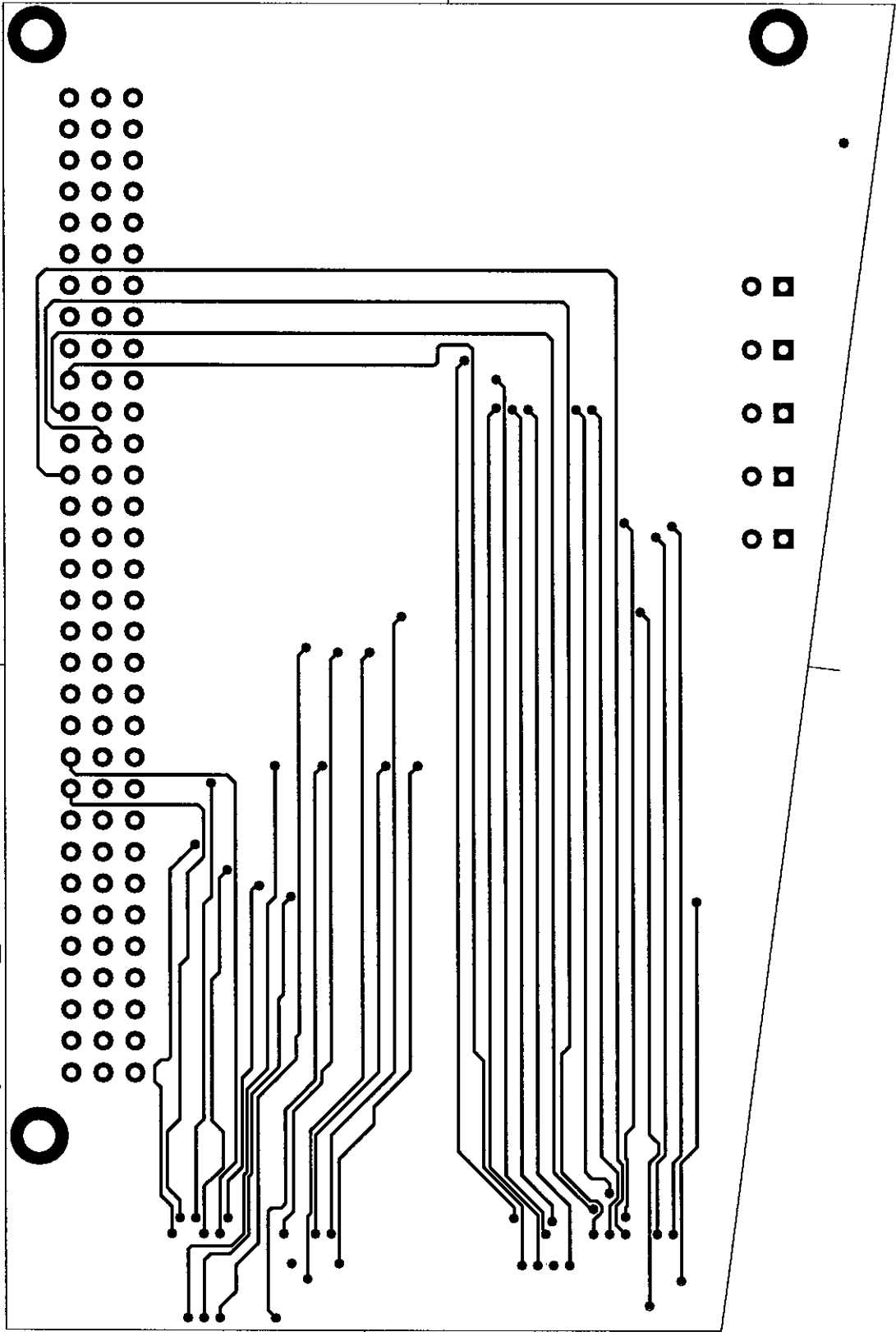
3 layers





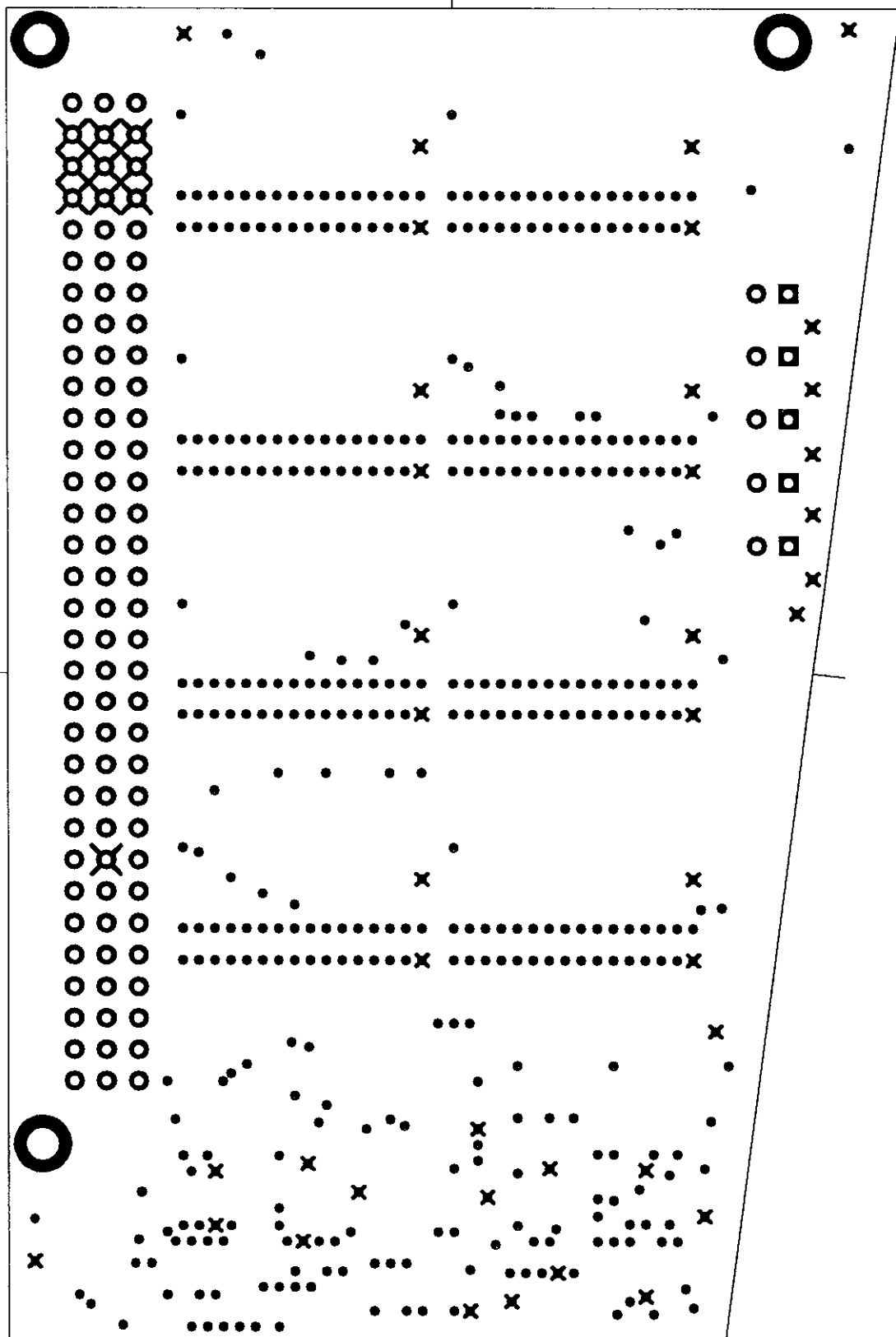
Layer 4

BOARD WAVE 3



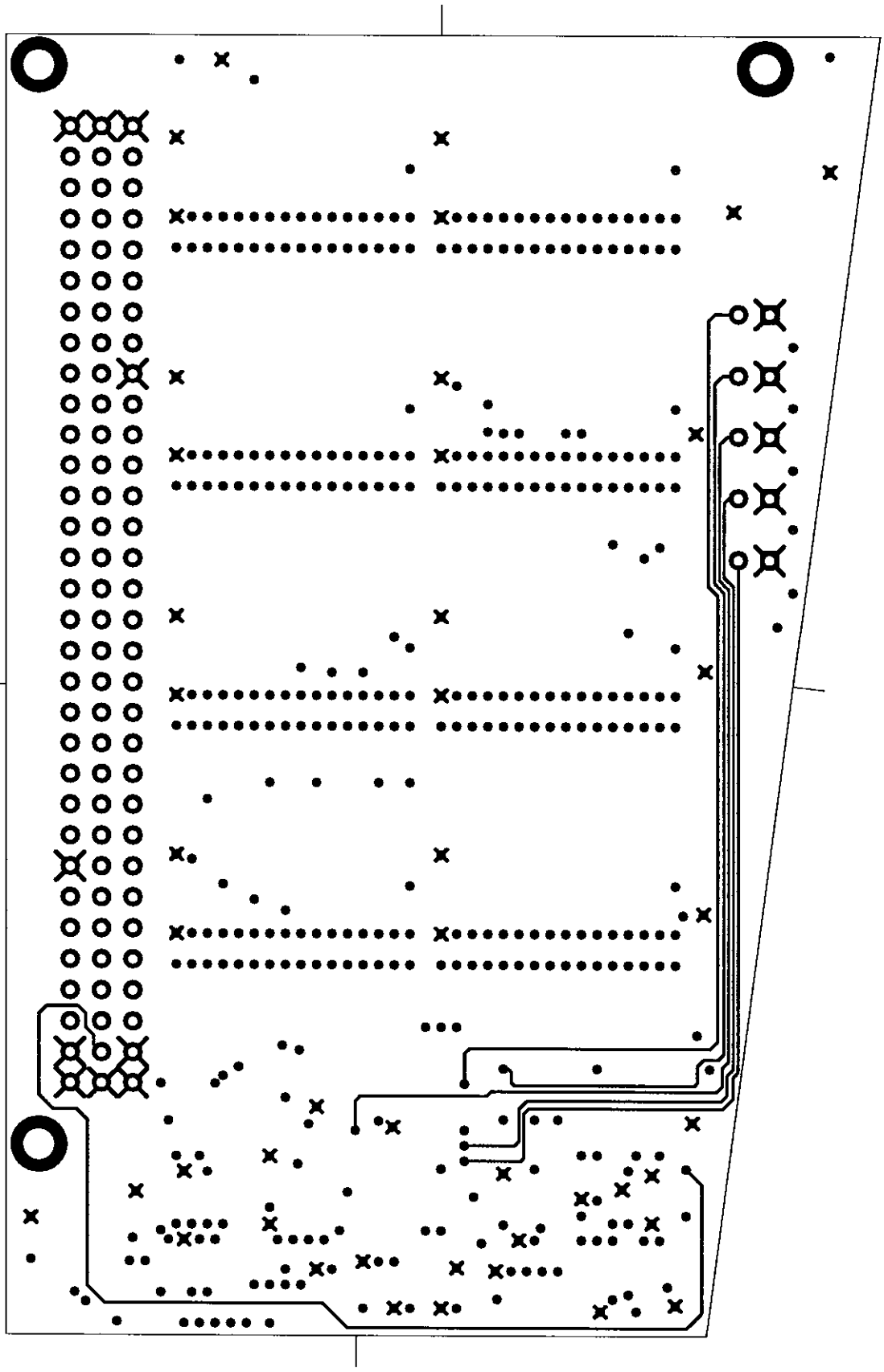
Layer 2

Board Layer 5



Layer 6

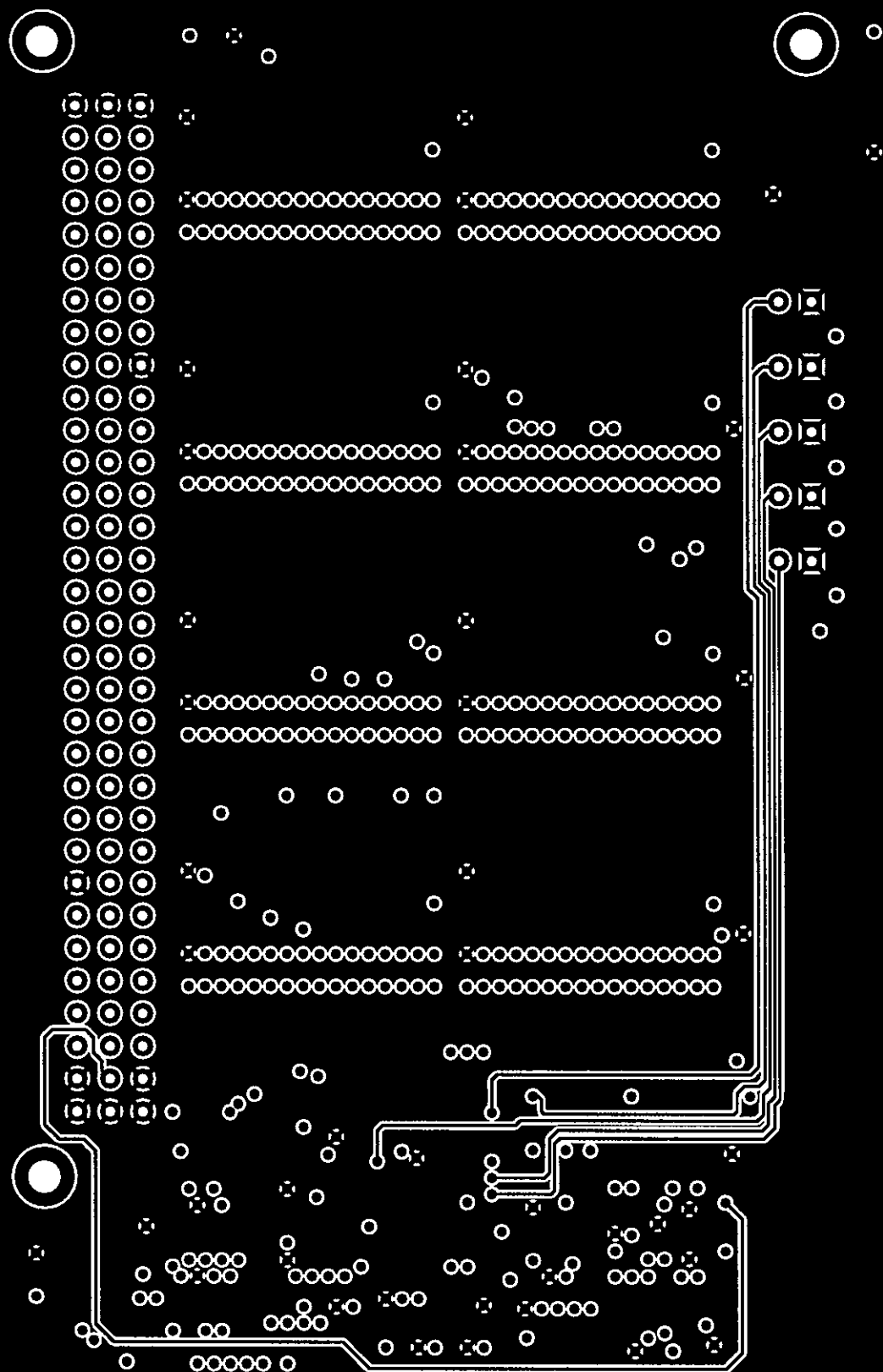
Board Layer 4
VCC

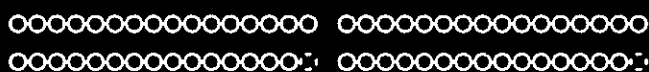
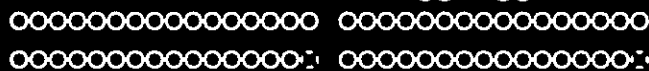
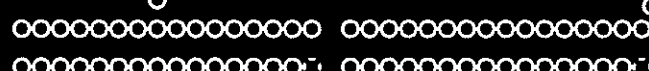


Layer 1

BOARD LAYERS
GND

Page 1

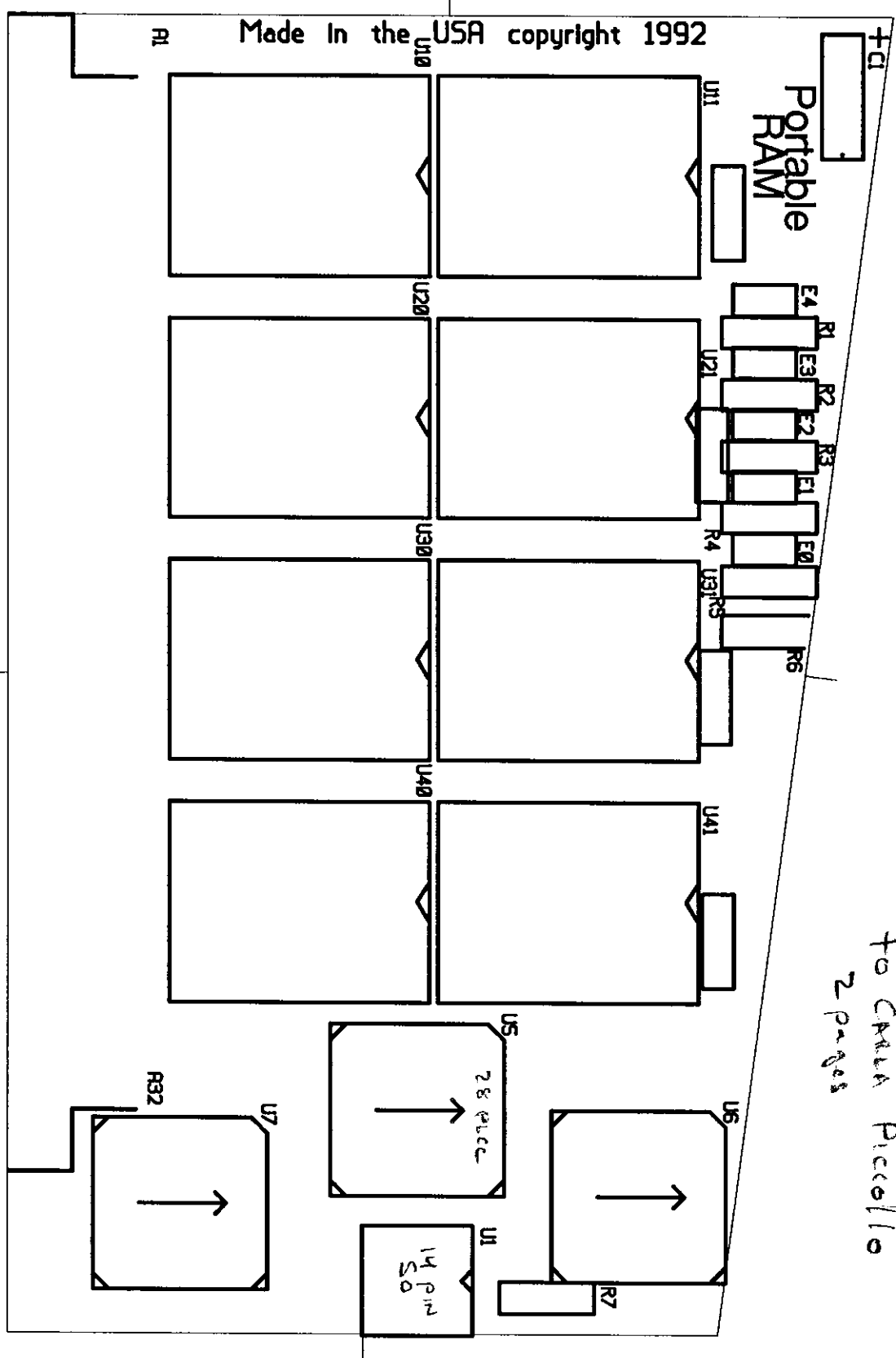




Layer 6



to CHAIN Piccolo
2 pages



Made In the USA copyright 1992

Portable RAM

Silkscreen component



□

1001

10

799

11/11/2016

1111

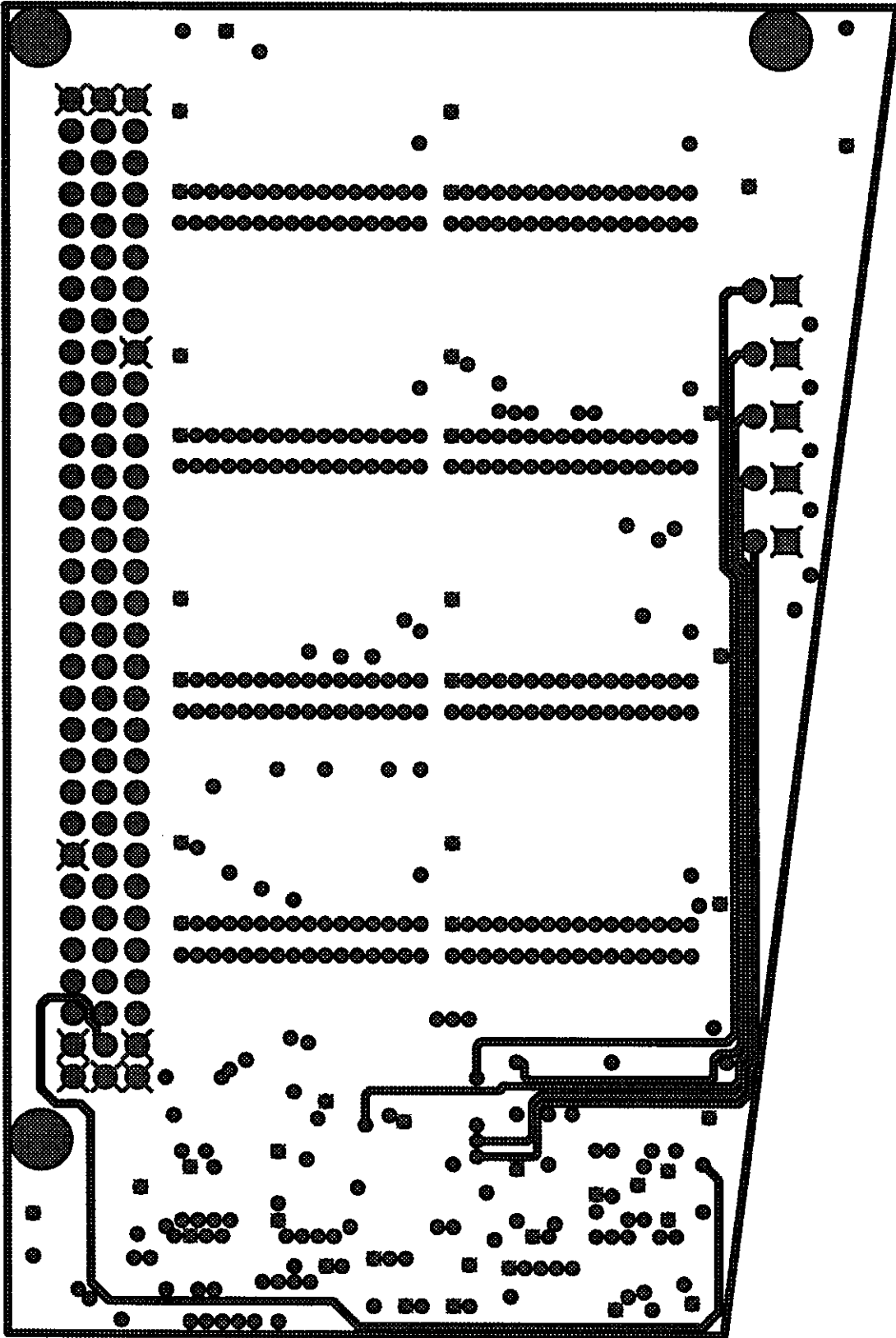
1561

111

באמצעות **האביר**

Ida

Figure 1



from the forward

Name
RAM,PLD;
Partno
Revision A;
Date
09/29/92;
Designer K LEISSES;
Company
Dynamic Engineering;
embly Portable RAM;
Location ;
Device
G22V101cc;
Format
J;

/* Inputs */
Pin 2 = spare1;
Pin [3..7]= [decoded..5];
Pin [9..12] = [a3..0];
Pin 13 = as;
Pin 16 = !r w;
Pin 17 = ~~!r w;~~

/* Outputs */
Pin 18 = ~~!r w;~~ S (P E C)
Pin 19 = !r1; /* not qualified with address strobe */
Pin 20 = !r2;
Pin 21 = !r3;
Pin 23 = !r4;
Pin 24 = !r5;
Pin 25 = !r6;
Pin 26 = !r7;
Pin 27 = !r8;

/* declarations */

old addr = [a3..0];
a3..0 corresponds to a23..a20 to bypass a CUPF feature *

/* Logic Equations */
/* qualify the spaces with AS and function codes to make sure we are in the user or super-space: */
/* the following equations are not qualified with as to be able to meet the timing */
/* required by the 68000. The last stage in the decoder pipeline is qualified */

r1 =
decoded1 & as & addr:1 /* ram bank 1, address 1 */
decoded2 & as & addr:2 /* ram bank 1, shifted from address 2 */
decoded3 & as & addr:3 /* ram bank 1, shifted from address 3 */
decoded4 & as & addr:4 /* ram bank 1, shifted from address 4 */
decoded5 & as & addr:5; /* ram bank 1, shifted from address 5 */

r2 =
decoded1 & as & addr:2 /* ram bank 2, address 2 */
decoded2 & as & addr:3 /* ram bank 2, shifted from address 3 */
decoded3 & as & addr:4 /* ram bank 2, shifted from address 4 */
decoded4 & as & addr:5 /* ram bank 2, shifted from address 5 */
decoded5 & as & addr:6; /* ram bank 2, shifted from address 6 */

r3 =
decoded1 & as & addr:3 /* ram bank 3, address 3 */
decoded2 & as & addr:4 /* ram bank 3, shifted from address 4 */
decoded3 & as & addr:5 /* ram bank 3, shifted from address 5 */
decoded4 & as & addr:6 /* ram bank 3, shifted from address 6 */
decoded5 & as & addr:7; /* ram bank 3, shifted from address 7 */

r4 =
decoded1 & as & addr:4 /* ram bank 4, address 4 */
decoded2 & as & addr:5 /* ram bank 4, shifted from address 5 */
decoded3 & as & addr:6 /* ram bank 4, shifted from address 6 */
decoded4 & as & addr:7 /* ram bank 4, shifted from address 7 */
decoded5 & as & addr:8; /* ram bank 4, shifted from address 8 */

r5 =
decoded1 & as & addr:5 /* ram bank 5, address 5 */
decoded2 & as & addr:6 /* ram bank 5, shifted from address 6 */
decoded3 & as & addr:7 /* ram bank 5, shifted from address 7 */

```

r6 = decoded1 & as & addr:6 /* ram bank 6, address 6 */
# decoded2 & as & addr:7 /* ram bank 6, shifted from address 7 */
# decoded3 & as & addr:8 /* ram bank 6, shifted from address 8 */
r7 = decoded1 & as & addr:7 /* ram bank 7, address 7 */
# decoded2 & as & addr:8 /* ram bank 7, shifted from address 8 */
r8 = decoded1 & as & addr:8 /* ram bank 8, address 8 */
r_w_u = decoded1 & as & uds: /* both UDS and R_W must be low for write upper to be

```

```

Name
Partno
Revision
Date
Designer
Company
Assembly
Location
Device
Format
J;
V7501cc;
U6;
Portable RAM;
Dynamic Engineering;
K LEISSES;
10/2/92;
A;
RFSHCNNTL;
RFSHCNNTL.PLD;

```

```

/* Inputs */
Pin 2 = |pwr_dwn;
Pin 3 = |clk;
Pin 4 = spare8;
Pin 5 = |i_o2 ;
Pin 6 = spare1;
Pin 7 = spare2;
Pin [9..12] = [spare3..6];
Pin 13 = |as;
Pin 16 = r_w;

```

```

/* Outputs */
Pin 17 = |oe_rfs;
Pin 18 = c0;
Pin 19 = |dtack;
Pin 20 = c5;
Pin 21 = c3;
Pin 23 = c4;
Pin 24 = c6;
Pin 25 = t0;
Pin 26 = t1;
Pin 27 = rfs;
rfs;

```

```

/* declarations */
Pinnode 30 = c2;
Pinnode 29 = c1;

```

```

Field astst = [t1..0];
Field state = [c6..0];

```

```

$define b0 'b'00
$define b1 'b'01
$define b2 'b'10
$define b3 'b'11

```

```

$define s0 'H'00
$define s1 'H'01
$define s2 'H'02
$define s3 'H'03
$define s4 'H'04
$define s5 'H'05
$define s6 'H'06
$define s7 'H'07
$define s8 'H'08
$define s9 'H'09
$define s10 'H'0A
$define s11 'H'0B
$define s12 'H'0C
$define s13 'H'0D
$define s14 'H'0E
$define s15 'H'0F
$define s16 'H'10
$define s17 'H'11
$define s18 'H'12
$define s19 'H'13
$define s20 'H'14

```

\$define s21 'H'15
\$define s22 'H'16
\$define s23 'H'17
\$define s24 'H'18
\$define s25 'H'19
\$define s26 'H'1A
\$define s27 'H'1B
\$define s28 'H'1C
\$define s29 'H'1D
\$define s30 'H'1E
\$define s31 'H'1F
\$define s32 'H'20
\$define s33 'H'21
\$define s34 'H'22
\$define s35 'H'23
\$define s36 'H'24
\$define s37 'H'25
\$define s38 'H'26
\$define s39 'H'27
\$define s40 'H'28
\$define s41 'H'29
\$define s42 'H'2A
\$define s43 'H'2B
\$define s44 'H'2C
\$define s45 'H'2D
\$define s46 'H'2E
\$define s47 'H'2F
\$define s48 'H'30
\$define s49 'H'31
\$define s50 'H'32
\$define s51 'H'33
\$define s52 'H'34
\$define s53 'H'35
\$define s54 'H'36
\$define s55 'H'37
\$define s56 'H'38
\$define s57 'H'39
\$define s58 'H'3A
\$define s59 'H'3B
\$define s60 'H'3C
\$define s61 'H'3D
\$define s62 'H'3E
\$define s63 'H'3F
\$define s64 'H'40
\$define s65 'H'41
\$define s66 'H'42
\$define s67 'H'43
\$define s68 'H'44
\$define s69 'H'45
\$define s70 'H'46
\$define s71 'H'47
\$define s72 'H'48
\$define s73 'H'49
\$define s74 'H'4A
\$define s75 'H'4B
\$define s76 'H'4C
\$define s77 'H'4D
\$define s78 'H'4E
\$define s79 'H'4F
\$define s80 'H'50
\$define s81 'H'51
\$define s82 'H'52
\$define s83 'H'53
\$define s84 'H'54
\$define s85 'H'55
\$define s86 'H'56

\$define s87 'H'57
\$define s88 'H'58
\$define s89 'H'59
\$define s90 'H'5A
\$define s91 'H'5B
\$define s92 'H'5C
\$define s93 'H'5D
\$define s94 'H'5E
\$define s95 'H'5F
\$define s96 'H'60
\$define s97 'H'61
\$define s98 'H'62
\$define s99 'H'63
\$define s100 'H'64
\$define s101 'H'65
\$define s102 'H'66
\$define s103 'H'67
\$define s104 'H'68
\$define s105 'H'69
\$define s106 'H'6A
\$define s107 'H'6B
\$define s108 'H'6C
\$define s109 'H'6D
\$define s110 'H'6E
\$define s111 'H'6F
\$define s112 'H'70
\$define s113 'H'71
\$define s114 'H'72
\$define s115 'H'73
\$define s116 'H'74
\$define s117 'H'75
\$define s118 'H'76
\$define s119 'H'77
\$define s120 'H'78
\$define s121 'H'79
\$define s122 'H'7A
\$define s123 'H'7B
\$define s124 'H'7C
\$define s125 'H'7D
\$define s126 'H'7E
\$define s127 'H'7F
\$define s128 'H'80
\$define s129 'H'81
\$define s130 'H'82
\$define s131 'H'83
\$define s132 'H'84
\$define s133 'H'85
\$define s134 'H'86
\$define s135 'H'87
\$define s136 'H'88
\$define s137 'H'89
\$define s138 'H'8A
\$define s139 'H'8B
\$define s140 'H'8C
\$define s141 'H'8D
\$define s142 'H'8E
\$define s143 'H'8F
\$define s144 'H'90
\$define s145 'H'91
\$define s146 'H'92
\$define s147 'H'93
\$define s148 'H'94
\$define s149 'H'95
\$define s150 'H'96
\$define s151 'H'97
\$define s152 'H'98

\$define s153 'H'99
\$define s154 'H'9A
\$define s155 'H'9B
\$define s156 'H'9C
\$define s157 'H'9D
\$define s158 'H'9E
\$define s159 'H'9F
\$define s160 'H'A0
\$define s161 'H'A1
\$define s162 'H'A2
\$define s163 'H'A3
\$define s164 'H'A4
\$define s165 'H'A5
\$define s166 'H'A6
\$define s167 'H'A7
\$define s168 'H'A8
\$define s169 'H'A9
\$define s170 'H'AA
\$define s171 'H'AB
\$define s172 'H'AC
\$define s173 'H'AD
\$define s174 'H'AE
\$define s175 'H'AF
\$define s176 'H'B0
\$define s177 'H'B1
\$define s178 'H'B2
\$define s179 'H'B3
\$define s180 'H'B4
\$define s181 'H'B5
\$define s182 'H'B6
\$define s183 'H'B7
\$define s184 'H'B8
\$define s185 'H'B9
\$define s186 'H'BA
\$define s187 'H'BB
\$define s188 'H'BC
\$define s189 'H'BD
\$define s190 'H'BE
\$define s191 'H'BF
\$define s192 'H'C0
\$define s193 'H'C1
\$define s194 'H'C2
\$define s195 'H'C3
\$define s196 'H'C4
\$define s197 'H'C5
\$define s198 'H'C6
\$define s199 'H'C7
\$define s200 'H'C8
\$define s201 'H'C9
\$define s202 'H'CA
\$define s203 'H'CB
\$define s204 'H'CC
\$define s205 'H'CD
\$define s206 'H'CE
\$define s207 'H'CF
\$define s208 'H'D0
\$define s209 'H'D1
\$define s210 'H'D2
\$define s211 'H'D3
\$define s212 'H'D4
\$define s213 'H'D5
\$define s214 'H'D6
\$define s215 'H'D7
\$define s216 'H'D8
\$define s217 'H'D9
\$define s218 'H'DA

```

$define s219 'H'DB
$define s220 'H'DC
$define s221 'H'DD
$define s222 'H'DE
$define s223 'H'DF
$define s224 'H'E0
$define s225 'H'E1
$define s226 'H'E2
$define s227 'H'E3
$define s228 'H'E4
$define s229 'H'E5
$define s230 'H'E6
$define s231 'H'E7
$define s232 'H'E8
$define s233 'H'E9
$define s234 'H'EA
$define s235 'H'EB
$define s236 'H'EC
$define s237 'H'ED
$define s238 'H'EE
$define s239 'H'EF
$define s240 'H'F0
$define s241 'H'F1
$define s242 'H'F2
$define s243 'H'F3
$define s244 'H'F4
$define s245 'H'F5
$define s246 'H'F6
$define s247 'H'F7
$define s248 'H'F8
$define s249 'H'F9
$define s250 'H'FA
$define s251 'H'FB
$define s252 'H'FC
$define s253 'H'FD
$define s254 'H'FE
$define s255 'H'FF

```

```

/* Logic Equations */
oe_rfsh = r_w # pwr_dwn # clk & astst:'b'10; /* output enable is inverted read writ
/* for standard access cycles. During sleep mode the OE_RFSH is held on */
/* with CE off for automatic refresh. The MacPortable supplies the power down*/
/* control signal */
/* OE_Refresh is turned on periodically for standard refresh. */

```

```

sequence astst {
  Present 'b'00 IF (ias)
  Present 'b'01 IF (as & !i_02 & rfsh_rqst)
  Default
  Next 'b'01;
  Next 'b'10;
  Next 'b'01;
  Next 'b'00;
  Next 'b'00;
  Next 'b'00;
}

```

```

rfsh_rqst = !clk & state:'H'FF & !rfsh_rqst # rfsh_rqst & !astst:'b'10;
rfsh_rqst.clk = clk;
t0.clk = clk;
t1.clk = clk;

```

```

sequence state {
  Present 'H'00 Next 'H'01;
  Present 'H'01 Next 'H'02;
  Present 'H'02 Next 'H'03;
  Present 'H'03 Next 'H'04;
  Present 'H'04 Next 'H'05;
  Present 'H'04 Next 'H'05;
  Present 'H'05 Next 'H'06;
  Present 'H'06 Next 'H'07;
}

```

Present	'H'07
Present	'H'08
Present	'H'09
Present	'H'0A
Present	'H'0B
Present	'H'0C
Present	'H'0D
Present	'H'0E
Present	'H'0F
Present	'H'10
Present	'H'11
Present	'H'12
Present	'H'13
Present	'H'14
Present	'H'15
Present	'H'16
Present	'H'17
Present	'H'18
Present	'H'19
Present	'H'1A
Present	'H'1B
Present	'H'1C
Present	'H'1D
Present	'H'1E
Present	'H'1F
Present	'H'20
Present	'H'21
Present	'H'22
Present	'H'23
Present	'H'24
Present	'H'25
Present	'H'26
Present	'H'27
Present	'H'28
Present	'H'29
Present	'H'2A
Present	'H'2B
Present	'H'2C
Present	'H'2D
Present	'H'2E
Present	'H'2F
Present	'H'30
Present	'H'31
Present	'H'32
Present	'H'33
Present	'H'34
Present	'H'35
Present	'H'36
Present	'H'37
Present	'H'38
Present	'H'39
Present	'H'3A
Present	'H'3B
Present	'H'3C
Present	'H'3D
Present	'H'3E
Present	'H'3F
Present	'H'40
Present	'H'41
Present	'H'42
Present	'H'43
Present	'H'44
Present	'H'45
Present	'H'46
Present	'H'47
Present	'H'48
Present	'H'49

Present 'H' 49
Next 'H' 4A
Present 'H' 4B
Next 'H' 4C
Present 'H' 4D
Next 'H' 4E
Present 'H' 4F
Next 'H' 50
Present 'H' 51
Next 'H' 52
Present 'H' 53
Next 'H' 54
Present 'H' 55
Next 'H' 56
Present 'H' 57
Next 'H' 58
Present 'H' 59
Next 'H' 5A
Present 'H' 5B
Next 'H' 5C
Present 'H' 5D
Next 'H' 5E
Present 'H' 5F
Next 'H' 60
Present 'H' 61
Next 'H' 62
Present 'H' 63
Next 'H' 64
Present 'H' 65
Next 'H' 66
Present 'H' 67
Next 'H' 68
Present 'H' 69
Next 'H' 6A
Present 'H' 6B
Next 'H' 6C
Present 'H' 6D
Next 'H' 6E
Present 'H' 6F
Next 'H' 70
Present 'H' 71
Next 'H' 72
Present 'H' 73
Next 'H' 74
Present 'H' 75
Next 'H' 76
Present 'H' 77
Next 'H' 78
Present 'H' 79
Next 'H' 7A
Present 'H' 7B
Next 'H' 7C
Present 'H' 7D
Next 'H' 7E
Present 'H' 7F
Next 'H' 80
Present 'H' 81
Next 'H' 82
Present 'H' 83
Next 'H' 84
Present 'H' 85
Next 'H' 86
Present 'H' 87
Next 'H' 88
Present 'H' 89
Next 'H' 8A
Present 'H' 8B
Next 'H' 8B

Present 'H' 8B
Next 'H' 8C
Present 'H' 8D
Next 'H' 8E
Present 'H' 8F
Next 'H' 90
Present 'H' 91
Next 'H' 92
Present 'H' 93
Next 'H' 94
Present 'H' 95
Next 'H' 96
Present 'H' 97
Next 'H' 98
Present 'H' 99
Next 'H' 9A
Present 'H' 9B
Next 'H' 9C
Present 'H' 9D
Next 'H' 9E
Present 'H' 9F
Next 'H' A0
Present 'H' A1
Next 'H' A2
Present 'H' A3
Next 'H' A4
Present 'H' A5
Next 'H' A6
Present 'H' A7
Next 'H' A8
Present 'H' A9
Next 'H' AA
Present 'H' AB
Next 'H' AC
Present 'H' AD
Next 'H' AE
Present 'H' AF
Next 'H' B0
Present 'H' B1
Next 'H' B2
Present 'H' B3
Next 'H' B4
Present 'H' B5
Next 'H' B6
Present 'H' B7
Next 'H' B8
Present 'H' B9
Next 'H' BA
Present 'H' BB
Next 'H' BC
Present 'H' BD
Next 'H' BE
Present 'H' BF
Next 'H' C0
Present 'H' C1
Next 'H' C2
Present 'H' C3
Next 'H' C4
Present 'H' C5
Next 'H' C6
Present 'H' C7
Next 'H' C8
Present 'H' C9
Next 'H' CA
Present 'H' CB
Next 'H' CC
Present 'H' CD

```

Present 'H'CD
Present 'H'CE
Present 'H'CF
Present 'H'D0
Present 'H'D1
Present 'H'D2
Present 'H'D3
Present 'H'D4
Present 'H'D5
Present 'H'D6
Present 'H'D7
Present 'H'D8
Present 'H'D9
Present 'H'DA
Present 'H'DB
Present 'H'DC
Present 'H'DD
Present 'H'DE
Present 'H'DF
Present 'H'E0
Present 'H'E1
Present 'H'E2
Present 'H'E3
Present 'H'E4
Present 'H'E5
Present 'H'E6
Present 'H'E7
Present 'H'E8
Present 'H'E9
Present 'H'EA
Present 'H'EB
Present 'H'EC
Present 'H'ED
Present 'H'EE
Present 'H'EF
Present 'H'F0
Present 'H'F1
Present 'H'F2
Present 'H'F3
Present 'H'F4
Present 'H'F5
Present 'H'F6
Present 'H'F7
Present 'H'F8
Present 'H'F9
Present 'H'FA
Present 'H'FB
Present 'H'FC
Present 'H'FD
Present 'H'FE
Present 'H'FF
Present
}
c0.clk = clk;
c1.clk = clk;
c2.clk = clk;
c3.clk = clk;
c4.clk = clk;
c5.clk = clk;
c6.clk = clk;
attack = 'b'0;
attack.oe = as & !o2;

```

Name
decoder.PLD;
Partno
decoder;
Revision
A;
Date
10/2/92;
Designer
K LEISSES;
Company
Dynamic Engineering;
embly
Location
;
Device
G22v101cc;
Format
J;

/* Inputs */
pin 2 = !pwrdsn;
pin 3 = sw4;
pin 4 = sw3;
pin {5..7} = {fc0..2};
pin {9..12} = {a3..0};
pin 13 = !as;
pin 16 = sw2;
pin 17 = sw1;
pin 18 = sw0;
/* Outputs */
pin 19 = !o2; /* not qualified with address strobe */
pin 20 = !decode1;
pin 21 = !decode2;
pin 23 = !decode3;
pin 24 = !decode4;
pin 25 = !decode5;
pin 26 = !i o; /* access to this board fully qualified */
pin 27 = !fc0_2;
/* decisions */

_ld addr = {a3..0};
/* a3..0 corresponds to a23..a20 to bypass a CPL feature */
field sw = {sw4..0};
/* create a field for the configuration switch setting */
/* Logic Equations */
/* qualify the spaces with AS and function codes to make sure we are in the user or super space. */
/* the follow equations are not qualified with as to be able to meet the timing */
/* required by the 68000. The last stage in the decoder pipeline is qualified */
fc0_2 = !fc0 # !fc1 # !fc2;

decoded2 = !pwrdsn & fc0_2 & ({sw:1 & addr:1})
(sw:2 & addr:1 # addr:2)
(sw:3 & addr:1..3)
(sw:4 & addr:1..4)
(sw:5 & addr:1..5)
(sw:6 & addr:1..6)
(sw:7 & addr:1..7)
(sw:8 & addr:1..8));

decoded3 = !pwrdsn & fc0_2 &
{sw:9 & addr:2..8}
{sw:A & addr:2..7}
{sw:B & addr:2..6}
{sw:C & addr:2..5}
{sw:D & addr:2..4}
{sw:E & addr:2..3}
{sw:F & addr:2});

_ode1 = !pwrdsn & fc0_2 &
{sw:H'10 & addr:3..8}
{sw:H'11 & addr:3..7}
{sw:H'12 & addr:3..6}
{sw:H'13 & addr:3..5}
{sw:H'14 & addr:3..4}
{sw:H'15 & addr:3});

```

decode4 = !pwrdsn & fc0_2 &
((sw:'H'16 & addr:[4..8])
# (sw:'H'17 & addr:[4..7])
# (sw:'H'18 & addr:[4..6])
# (sw:'H'19 & addr:[4..5])
# (sw:'H'1A & addr:[4])?)

decode5 = !pwrdsn & fc0_2 &
((sw:'H'1B & addr:[5..8])
# (sw:'H'1C & addr:[5..7])
# (sw:'H'1D & addr:[5..6])
# (sw:'H'1E & addr:[5])?)

!_o = as & (decode1 # decode2 # decode3 # decode4 # decode5)
!_o2 = (decode1 # decode2 # decode3 # decode4 # decode5)
/* caution !_o2 is not fully decoded -- must be qualified with as */

```