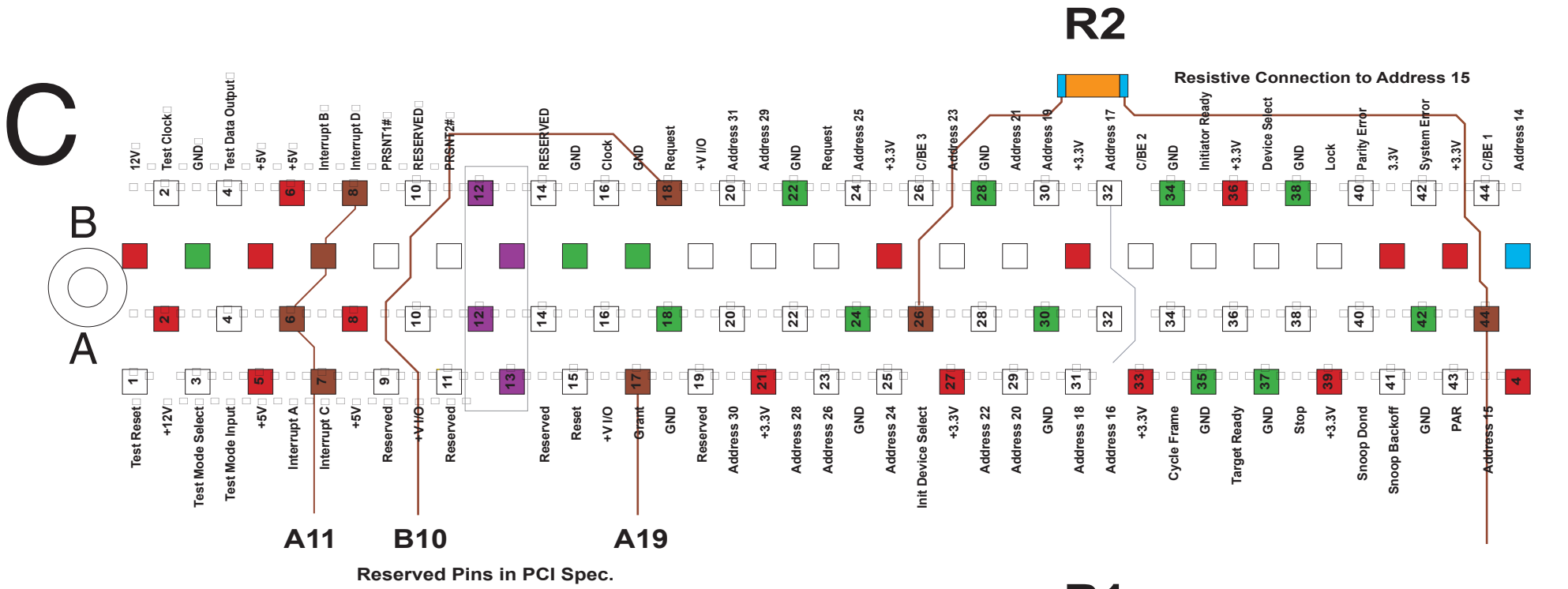
C
B
A
R2
Resistive Connection to Address 15
12V
Test Clock
GND
Test Data Output
+5V
+5V
Interrupt B
Interrupt D
PRSNT1#
RESERVED
PRSNT2#
RESERVED
GND
Clock
GND
Request
+V I/O
Address 31
Address 29
GND
Request
Address 25
+3.3V
C/BE 3
Address 23
GND
Address 21
Address 19
+3.3V
Address 17
C/BE 2
GND
Initiator Ready
+3.3V
Device Select
GND
Lock
Parity Error
3.3V
System Error
+3.3V
C/BE 1
Address 14
Test Reset
+12V
Test Mode Select
Test Mode Input
+5V
Interrupt A
Interrupt C
+5V
Reserved
+V I/O
Reserved
Reserved
Reset
+V I/O
Grant
GND
Reserved
Address 30
+3.3V
Address 28
Address 26
GND
Address 24
Init Device Select
+3.3V
Address 22
Address 20
GND
Address 18
Address 16
+3.3V
Cycle Frame
GND
Target Ready
GND
Stop
+3.3V
Snoop Dond
Snoop Backoff
GND
PAR
Address 15
A11
B10
A19
Reserved Pins in PCI Spec.
B
A
R1
Resistive Connection to Address 14
A9
B14
A14
Reserved Pins in PCI Spec.
Test_Cable_Patch-220.PDF