

Z86E40

CMOS Z8® OTP CCP™ MICROCONTROLLER

FEATURES

- 8-Bit CMOS Microcontroller
- 40-Pin DIP or 44-Pin PLCC Package
- Low Cost
- 4.5V to 5.5V Operating Range
- Software Programmable Low EMI Mode.
- Pull-Up Active/Open-Drain Programmable on Port 0, Port 1 and Port 2
- EPROM Protect Programmable
- RAM Protect Programmable
- RC Oscillator Programmable
- Low Power Consumption - 60 mW
- Fast Instruction Pointer - 0.6 μ s
- Two standby modes - STOP and HALT
- 32 Input/Output Lines
- Digital Inputs CMOS Levels, Schmitt-Triggered
- 4 Kbytes of One-Time PROM
- 236 Bytes of RAM
- Three Expanded Register File Control Registers
- Two Programmable 8-Bit Counter/Timers each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Clock Speeds up to 12 MHz
- Watch-Dog Timer
- Auto Power-On Reset
- Two Comparators
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.

10

GENERAL DESCRIPTION

The Z86E40 Consumer Controller Processor (CCP™) introduces a new level of sophistication to single-chip architecture. The Z86E40 is a member of the Z8® single-chip microcontroller family with 4 Kbytes of EPROM and 236 bytes of RAM. The device is housed in a 40-pin DIP, 44-pin PLCC, and a 44-pin Quad Flat Pack, and is manufactured in CMOS technology. The device offers easy software development and debug, prototyping, and small production runs not economically desirable with a masked ROM version.

The Z86E40 architecture is characterized by Zilog's 8-bit microcontroller core with an expanded register file to allow easy access to register mapped peripheral and I/O cir-

cuits. The CCP offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many industrial, consumer, automotive, peripheral types, and advanced scientific applications.

The Z86E40 has 32 pins dedicated to input and output for applications demanding powerful I/O capabilities. These lines are grouped into four ports, eight lines per port, and are configurable under software control to provide timing, status signals, and parallel I/O with or without handshake, and address/data bus for interfacing external memory.

GENERAL DESCRIPTION (Continued)

There are four basic address spaces available to support this wide range of configurations: Program Memory, Data Memory, Register File, and Expanded Register File (ERF). The Register File is composed of 236 bytes of general-purpose registers, four I/O port registers, and 15 control and status registers. The Expanded Register File consists of three control registers.

To unburden the program from coping with the real-time problems such as counting/timing and input/output data communication, the Z86E40 offers two on-chip counter/timers with a large number of user selectable modes, and two on-board comparators to process analog signals with a common reference voltage (Figures 1 and 2).

Notes:

All Signals with a preceding front slash, "/", are active Low, e.g., B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power Ground	V _{CC} GND	V _{DD} V _{SS}

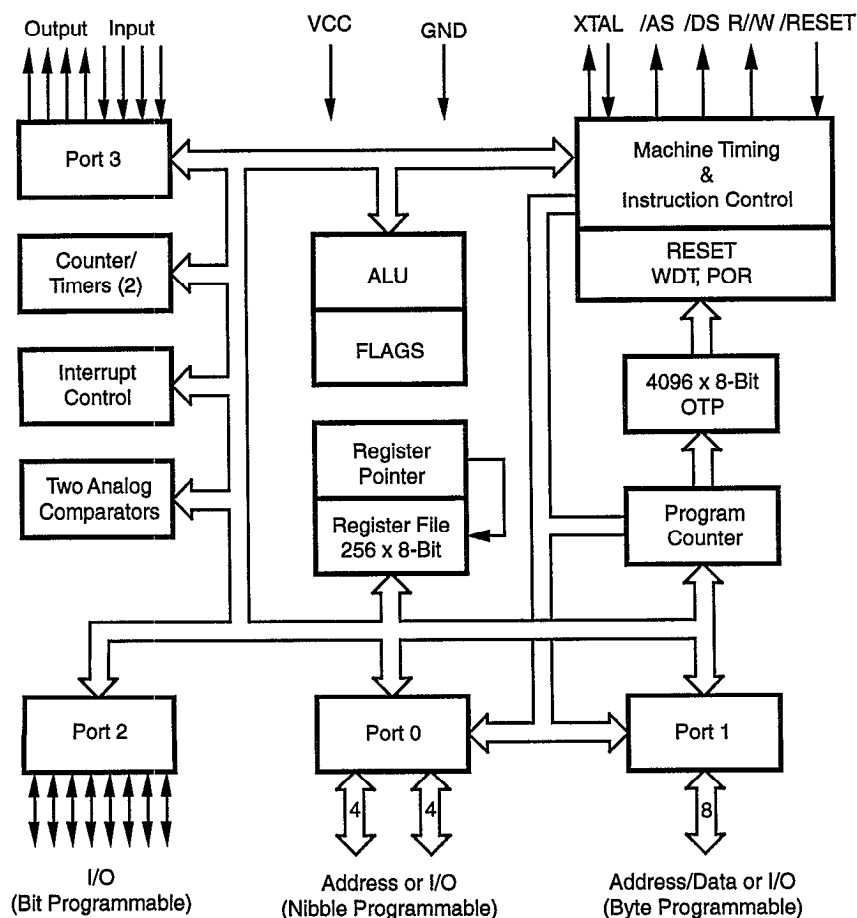


Figure 1. Functional Block Diagram

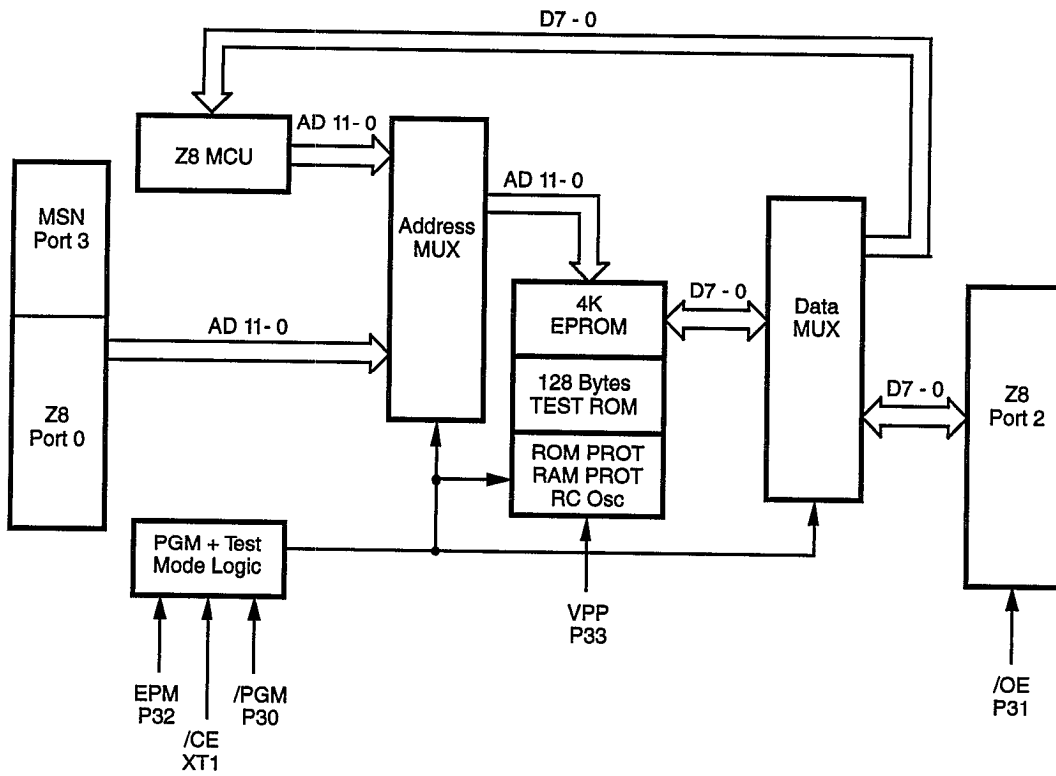
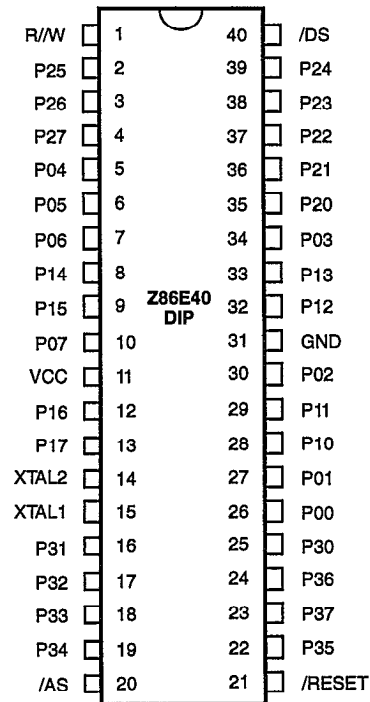
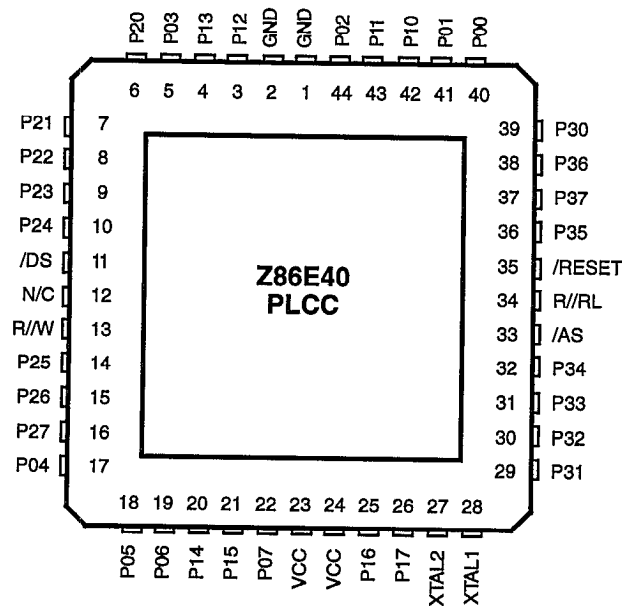


Figure 2. EPROM Programming Block Diagram

10

PIN IDENTIFICATION

Figure 3. 40-Pin DIP Pin Assignments (Standard Mode)
Table 1. 40-Pin DIP Pin Identification (Standard Mode)

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	R/W	Read/Write	Output	22	P35	Port 3, Pin 5	Output
2-4	P25-P27	Port 2, Pins 5,6,7	In/Output	23	P37	Port 3, Pin 7	Output
5-7	P04-P06	Port 0, Pins 4,5,6	In/Output	24	P36	Port 3, Pin 6	Output
8-9	P14-P15	Port 1, Pins 4,5	In/Output	25	P30	Port 3, Pin 0	Input
10	P07	Port 0, Pin 7	In/Output	26-27	P00-P01	Port 0, Pins 0,1	In/Output
11	V _{cc}	Power Supply		28-29	P10-P11	Port 1, Pins 0,1	In/Output
12-13	P16-P17	Port 1, Pins 6,7	In/Output	30	P02	Port 0, Pin 2	In/Output
14	XTAL2	Crystal Oscillator	Output	31	GND	Ground	
15	XTAL1	Crystal Oscillator	Input	32-33	P12-P13	Port 1, Pins 2,3	In/Output
16-18	P31-P33	Port 3, Pins 1,2,3	Input	34	P03	Port 0, Pin 3	In/Output
19	P34	Port 3, Pin 4	Output	35-39	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output
20	/AS	Address Strobe	Output	40	/DS	Data Strobe	Output
21	/RESET	Reset	Input				

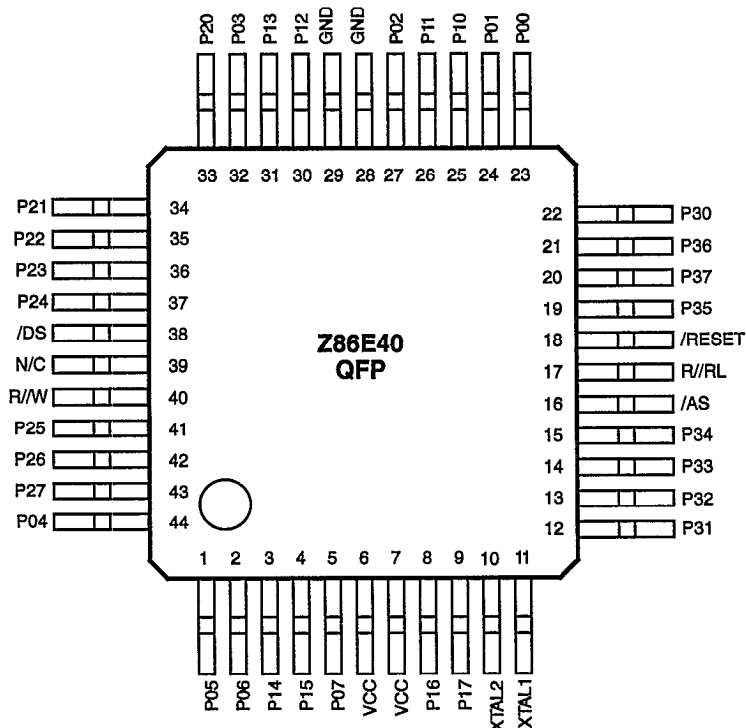


10

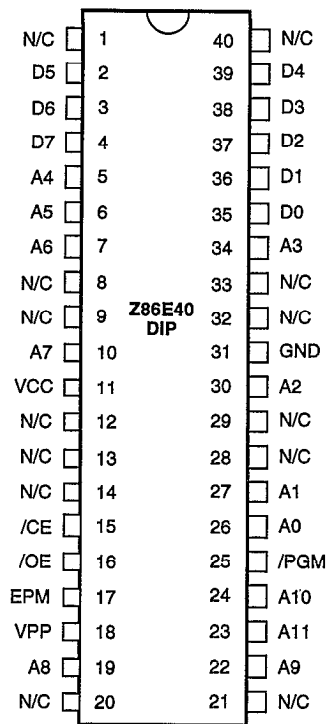
Figure 4. 44-Pin PLCC Pin Assignments (Standard Mode)

Table 2. 44-Pin Plastic Leaded Chip Carrier Pin Identification (Standard Mode)

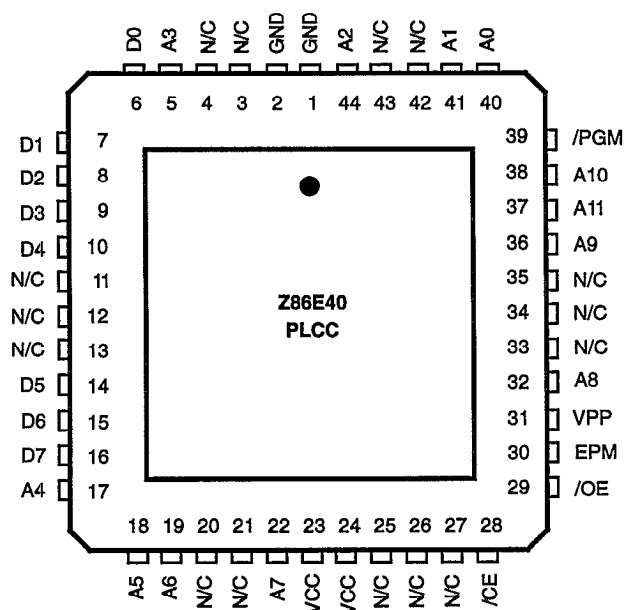
Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-2	GND	Ground		28	XTAL1	Crystal Oscillator	Input
3-4	P12-P13	Port 1, Pins 2,3	In/Output	29-31	P31-P33	Port 3, Pins 1,2,3	Input
5	P03	Port 0, Pin 3	In/Output	32	P34	Port 3, Pin 4	Output
6-10	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output	33	/AS	Address Strobe	Output
11	/DS	Data Strobe	Output	34	R//RL	ROM/ROMless select	Input
12	N/C	No Connection		35	/RESET	Reset	Input
13	R//W	Read/Write	Output	36	P35	Port 3, Pin 5	Output
14-16	P25-P27	Port 2, Pins 5,6,7	In/Output	37	P37	Port 3, Pin 7	Output
17-19	P04-P06	Port 0, Pins 4,5,6	In/Output	38	P36	Port 3, Pin 6	Output
20-21	P14-P05	Port 1, Pins 4,5	In/Output	39	P30	Port 3, Pin 0	Input
22	P07	Port 0, Pin 7	In/Output	40-41	P00-P01	Port 0, Pins 0,1	In/Output
23-24	V _{cc}	Power Supply		42-43	P10-P11	Port 1, Pins 0,1	In/Output
25-26	P16-P17	Port 1, Pins 6,7	In/Output	44	P02	Port 0, Pin 2	In/Output
27	XTAL2	Crystal Oscillator	Output				

PIN IDENTIFICATION (Continued)

Figure 5. 44-Pin QFP Pin Assignments (Standard Mode)
Table 3. 44-Pin QFP Pin Identification (Standard Mode)

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-2	P05-P06	Port 0, Pins 5,6	In/Output	21	P36	Port 3, Pin 6	Output
3-4	P14-P05	Port 1, Pins 4,5	In/Output	22	P30	Port 3, Pin 0	Input
5	P07	Port 0, Pin 7	In/Output	23-24	P00-P01	Port 0, Pin 0,1	In/Output
6-7	V _{cc}	Power Supply		25-26	P10-P11	Port 1, Pins 0,1	In/Output
8-9	P16-P17	Port 1, Pins 6,7	In/Output	27	P02	Port 0, Pin 2	In/Output
10	XTAL2	Crystal Oscillator	Output	28-29	GND	Ground	
11	XTAL1	Crystal Oscillator	Input	30-31	P12-P13	Port 1, Pins 2,3	In/Output
12-14	P31-P13	Port 3, Pins 1,2,3	Input	32	P03	Port 0, Pin 3	In/Output
15	P34	Port 3, Pin 4	Output	33-37	P20-4	Port 2, Pins 0,1,2,3,4	In/Output
16	/AS	Address Strobe	Output	38	/DS	Data Strobe	Output
17	R//RL	ROM/ROMless select	Input	39	N/C	No Connection	
18	/RESET	Reset	Input	40	R//W	Read/Write	Output
19	P35	Port 3, Pin 5	Output	41-43	P25-P27	Port 2, Pins 5,6,7	In/Output
20	P37	Port 3, Pin 7	Output	44	P04	Port 0, Pin 4	In/Output


10
Figure 6. 40-Pin DIP Pin Assignments (EPROM Programming Mode)
Table 4. 40-Pin DIP Package Pin Identification (EPROM Programming Mode)

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1	N/C	No Connection		22	A9	Address 9	Input
2-4	D5-D7	Data 5,6,7	In/Output	23	A11	Address 11	Input
5-7	A4-A6	Address 4,5,6	Input	24	A10	Address 10	Input
8-9	N/C	No Connection		25	/PGM	Prog. Mode	Input
10	A7	Address 7	Input	26-27	A0-A1	Address 0,1	Input
11	V _{cc}	Power Supply		28-29	N/C	No Connection	
12-14	N/C	No Connection		30	A2	Address 2	Input
15	/CE	Chip Select	Input	31	GND	Ground	
16	/OE	Output Enable	Input	32-33	N/C	No Connection	
17	EPM	EPROM Prog. Mode	Input	34	A3	Address 3	Input
18	V _{pp}	Prog. Voltage	Input	35-39	D0-D4	Data 0,1,2,3,4	In/Output
19	A8	Address 8	Input	40	N/C	No Connection	
20-21	N/C	No Connection					

PIN IDENTIFICATION (Continued)

Figure 7. 44-Pin PLCC Pin Assignments (EPROM programming mode)
Table 5. 44-Pin Leaded Chip Carrier Pin Identification (EPROM Programming Mode)

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-2	GND	Ground		29	/OE	Output Enable	Input
3-4	N/C	No Connection		30	EPM	EPROM Prog. Mode	Input
5	A3	Address 3	Input	31	V _{PP}	Prog. Voltage	Input
6-10	D0-D4	Data 0,1,2,3,4	In/Output	32	A8	Address 8	Input
11-13	N/C	No Connection		33-35	N/C	No Connection	
14-16	D5-D7	Data 5,6,7	In/Output	36	A9	Address 9	Input
17-19	A4-A6	Address 4,5,6	Input	37	A11	Address 11	Input
20-21	N/C	No Connection		38	A10	Address 10	Input
22	A7	Address 7	Input	39	/PGM	Prog. Mode	Input
23-24	V _{CC}	Power Supply		40-41	A0,A1	Address 0,1	Input
25-27	N/C	No Connection		42-43	N/C	No Connection	
28	/CE	Chip Select	Input	44	A2	Address 2	Input

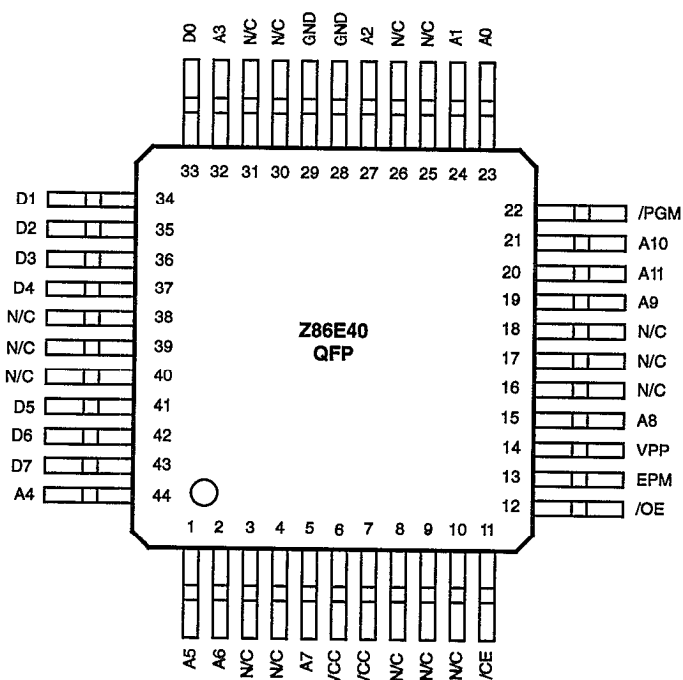


Figure 8. 44-Pin QFP Pin Assignments (EPROM programming mode)

Table 6. 44-pin Quad Flat Pack (EPROM Programming Mode)

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1-2	A5-A6	Address 5,6	Input	21	A10	Address 10	Input
3-4	N/C	No Connection		22	/PGM	Prog. Mode	Input
5	A7	Address 7	Input	23-24	A0,A1	Address 0,1	Input
6-7	V _{CC}	Power Supply		25-26	N/C	No Connection	
8-10	N/C	No Connection		27	A2	Address 2	Input
11	/CE	Chip Select	Input	28-29	GND	Ground	
12	/OE	Output Enable	Input	30-31	N/C	No Connection	
13	EPM	EPROM Prog. Mode	Input	32	A3	Address 3	Input
14	V _{PP}	Prog. Voltage	Input	33-37	D0-D4	Data 0,1,2,3,4	In/Output
15	A8	Address 8	Input	38-40	N/C	No Connection	
16-18	N/C	No Connection		41-43	D5-D7	Data 5,6,7	In/Output
19	A9	Address 9	Input	44	A4	Address 4	Input
20	A11	Address 11	Input				

PIN FUNCTIONS

EPROM Programming Mode

D7-D0 Data Bus. The data can be read from or written to external memory through the data bus.

A11-A0 Address Bus. During programming, the EPROM address is written to the address bus.

V_{cc} Power Supply. This pin has to supply 5V during the EPROM read mode and 6V during other modes.

/CE Chip Enable (active Low). This pin is active during EPROM Read Mode, Program Mode and Program Verify Mode.

/OE Output Enable (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output. When High, the Data Bus is input.

EPM EPROM Program Mode. This pin controls the different EPROM Program Mode by applying different voltages.

V_{pp} Program Voltage. This pin supplies the program voltage.

/PGM Program Mode (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

Application Precaution

The production test-mode environment may be enabled accidentally during normal operation if **excessive noise** surges above V_{cc} occur on the following specific pins:

XTAL1 pin
/RESET pin.

In addition, processor operation of Z8 One-Time Programmable devices may be affected by excessive noise surges on the V_{pp}, /CE, /EPM, /OE pins while the microcontroller is in standard mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

Using a clamping diode to V_{cc}

Adding a capacitor to the affected pin.

Z86E40 Standard Mode

XTAL Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network, or external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network to the on-chip oscillator output.

R/W Read/Write (output, write Low). The R/W signal is Low when the CCP is writing to the external program or data memory.

/RESET Reset (input, active Low). Reset will initialize the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer reset, Stop-Mode Recovery, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin low for the POR time. Any devices driving the reset line must be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull up is provided internally. After the POR time, /RESET is a Schmitt-triggered input.

To avoid asynchronous and noisy reset problems, the Z86E40 is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000CH, 5-10 TpC cycles after /RESET is released. For Power-On Reset, the reset output time is 5 ms. The Z86E40 does not reset WDTMR, SMR, P2M, and P3M registers on a Stop-Mode Recovery operation.

Port 0 (P07-P00). Port 0 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The input buffers are Schmitt-triggered and nibble programmed. Either nibble output that can be globally programmed as push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can be

placed under handshake control. In Handshake mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 provides address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the

lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. In ROMless mode, after a hardware reset, Port 0 is configured as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode. In ROM mode, Port 0 is defined as input after reset.

Port 0 can be set in the high-impedance mode if selected as an address output state, along with Port 1 and the control signals /AS, /DS, and R/W (Figure 9).

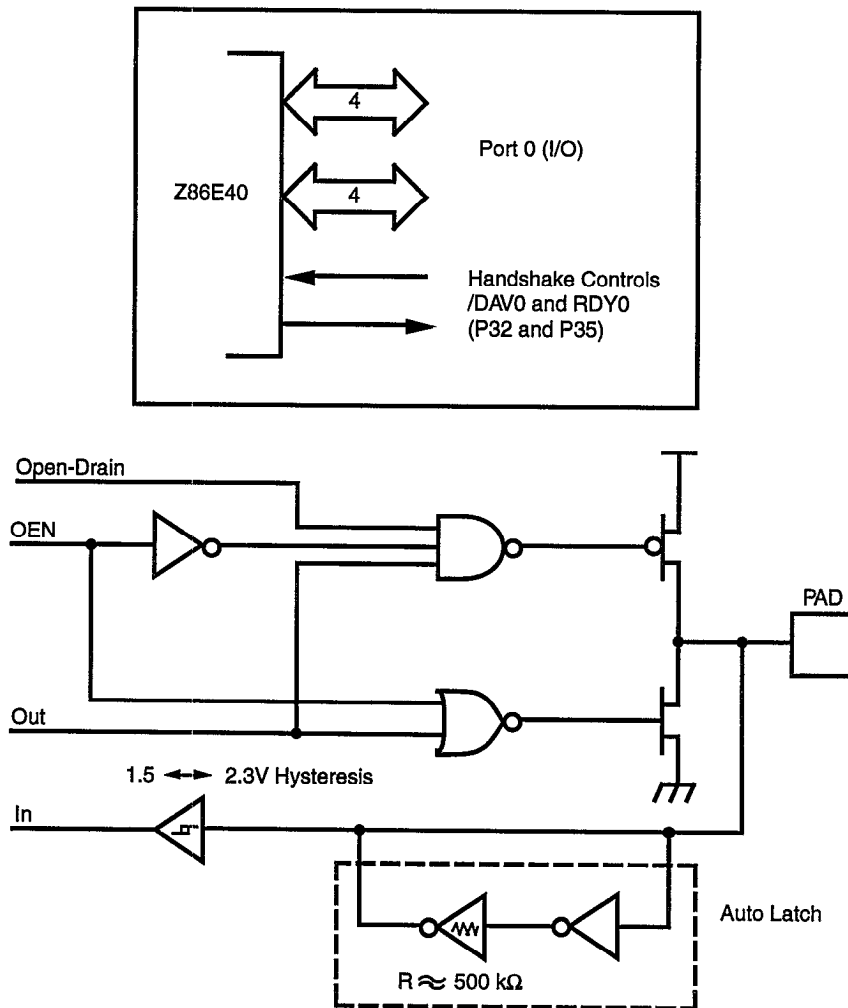


Figure 9. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17-P10). Port 1 is an 8-bit, bidirectional, CMOS compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports. These eight I/O lines can be programmed as inputs or outputs or can be configured under software control as an Address/Data port for interfacing external memory. The input buffers are Schmitt triggered and the output buffers can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 1 can be placed under handshake control. In this configuration, Port 3, lines P33 and P34 are used as the handshake

controls RDY1 and /DAV1 (Ready and Data Available). To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 outputs the additional lines (Figure 10).

Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS, and R/W, allowing the Z86E40 to share common resources in multiprocessor and DMA applications.

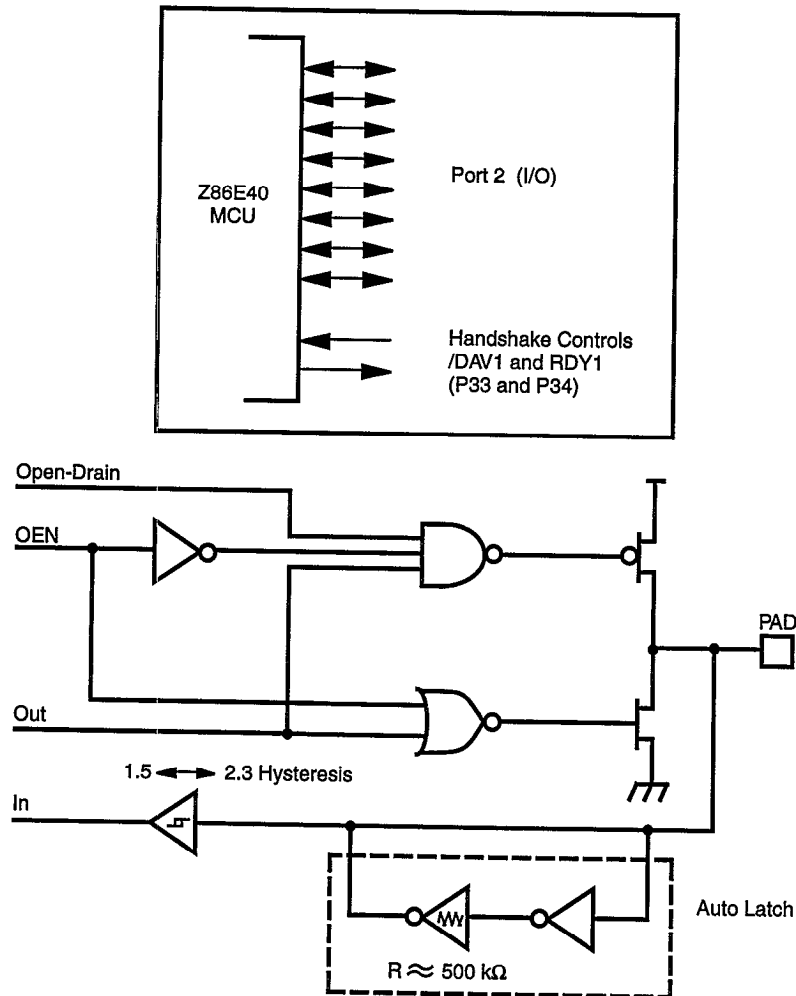


Figure 10. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control.

In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (Figure 11).

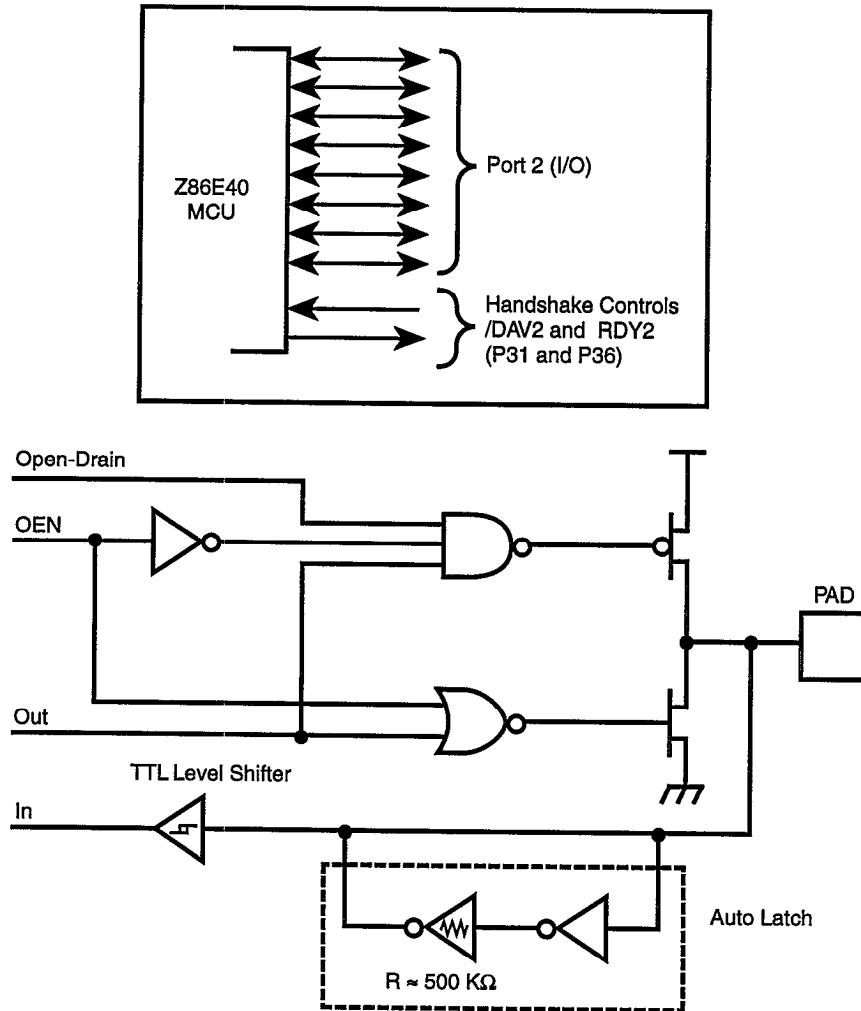


Figure 11. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port3 (P37-P30). Port 3 is an 8-bit, CMOS compatible port with four fixed input and four fixed output. Port 3 consists of four fixed input (P33-P30), and four fixed output (P37-P34), and can be configured by software for interrupt and handshake control functions. Port 3, Pin 0 is Schmitt-triggered. P31, P32 and P33 are standard CMOS inputs (no Auto Latches) and P34, P35, P36 and P37 are push-pull output lines. Low EMI output buffers can be globally programmed by the software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by setting the D1 of Port 3 Mode Register (P3M). The comparator output can be outputted from P34 and P37, respec-

tively, by setting PCON register Bit D0 to 1 state. For the interrupt function, P30 and P33 are falling edge triggered interrupt inputs. P31 and P32 can be programmed as falling, rising or both edges triggered interrupt inputs (Figure 12). Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Port 0, Port 1, and Port 2 are also available on Port 3 (Table 7).

Note: P33-P30 differs from the Z86C40 because there is no clamping diode to V_{CC} due to the EPROM high-voltage circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode.

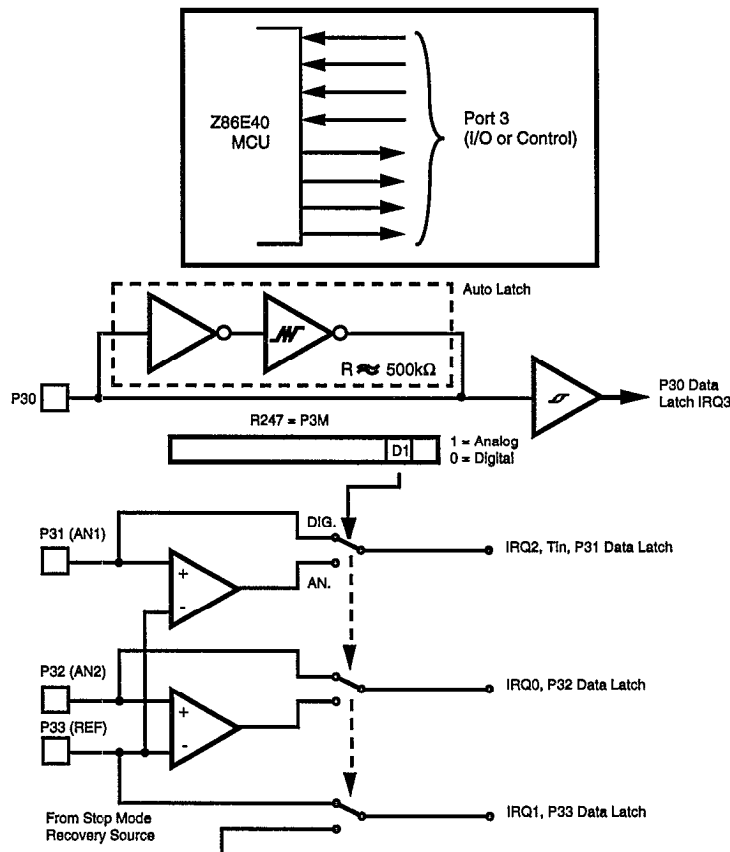


Figure 12. Port 3 Configuration

Table 7. Pin Assignments of Port 3

Pin	I/O	CTC1	Analog	Interrupt	P0 HS	P1 HS	P2 HS	Ext
P30	IN	T _{IN}		IRQ3				
P31	IN		AN1	IRQ2		D/R		
P32	IN		AN2	IRQ0	D/R			
P33	IN		REF	IRQ1		D/R		
P34	OUT	T _{OUT}	AN1-Out					R/D
	/DM							
P35	OUT				R/D			
P36	OUT					R/D		
P37	OUT		An2-Out					

Comparator Inputs. Port 3 P31 and P32 each has a comparator front end. The comparator reference voltage P33 is common to both comparators. In analog mode, P31 and P32 are the positive input of the comparators and P33 is the reference voltage of the comparators.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33-P31) that are not externally driven. Whether this level is zero or one, cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Auto Latches are available on Port 0, Port 2 and P30. There are no Auto Latches on P31, P32, and P33.

Low EMI Emission. The Z86E40 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate is reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 Ohms (typical).
- Oscillator divide-by-two circuitry is eliminated.
- Internal SLCK/TCLK = XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time.

10

FUNCTIONAL DESCRIPTION

The Z8 CCP incorporates special functions to enhance the Z8's applications in industrial, scientific research, and advanced technologies applications.

RESET. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source

Having the Auto Power-on Reset circuitry built-in, the Z86E40 does not need to be connected to an external power-on reset circuit. The reset time is 5 ms (typical) plus 18 clock cycles. The Z86E40 does not re-initialize WDTMR,

SMR, P2M, and P3M registers to their reset values on a Stop-Mode Recovery operation. Note: The device V_{CC} must rise up to the operating V_{CC} specification before the T_{POR} expires.

Program Memory. The Z86E40 can address up to 4 Kbytes of internal program memory (Figure 13). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM mode, byte 12 (000CH) to address 4095 (0FFFH) consists of programmable EPROM. After reset, the program counter points at the address 000CH which is the starting address of the user program. In ROMless mode, the Z86E40 can address up to 64 Kbytes of external program memory. The ROM/ROMless option is only available on the 44-pin devices.

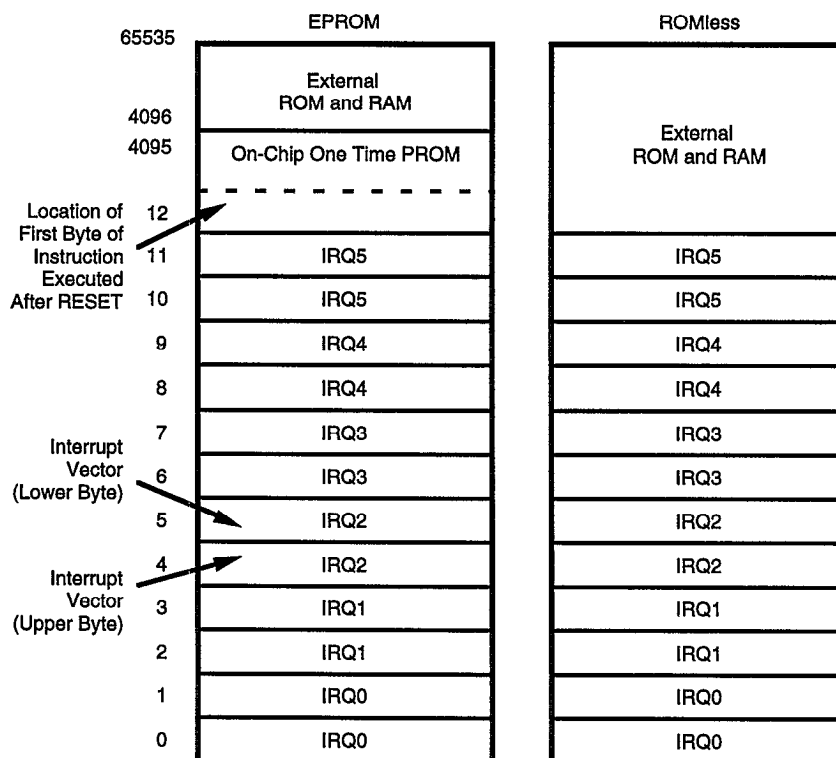


Figure 13. Program Memory Map

EPROM Protect. The 4 Kbytes of program memory is a one-time PROM. **An EPROM protect feature prevents dumping of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions to program memory in all modes.** ROM look-up tables cannot be used with this feature.

Data Memory (/DM). In EPROM mode, the Z86E40 can address up to 60 Kbytes of external data memory beginning at location 4096. In ROMless mode, the Z86E40 can

address up to 64 Kbytes of data memory. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 14). The state of the /DM signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory.

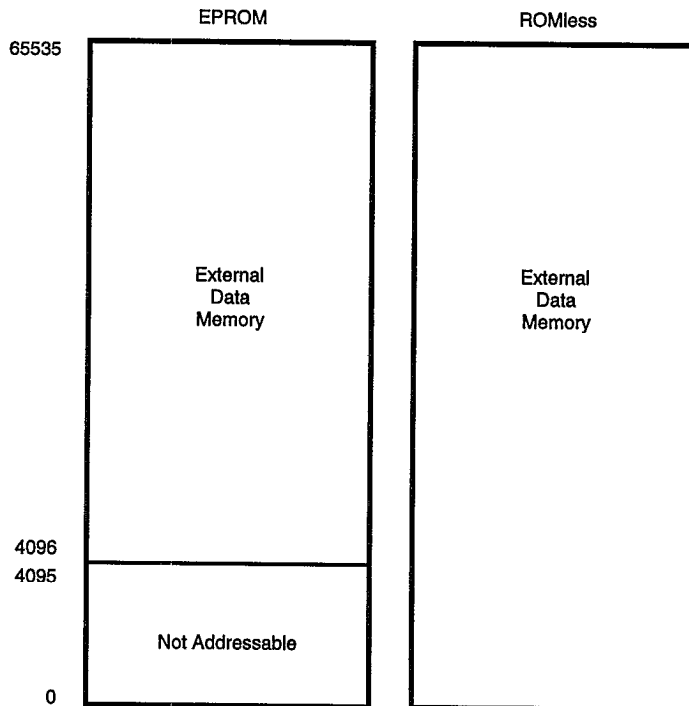


Figure 14. Data Memory Map

Expanded Register File. The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 15). These register groups are known as the Expanded Register File (ERF).

The low nibble (D3-D0) of the Register Pointer (RP) select the active ERF group, and the high nibble (D7-D4) of register RP select the working register group (Figure 16). Three system configuration registers reside in the Expanded Register File at bank FH: PCON, SMR, and WDTMR. The rest of the Expanded Register is not physically implemented and is reserved for future expansion.

FUNCTIONAL DESCRIPTION (Continued)

Z8 STANDARD CONTROL REGISTERS

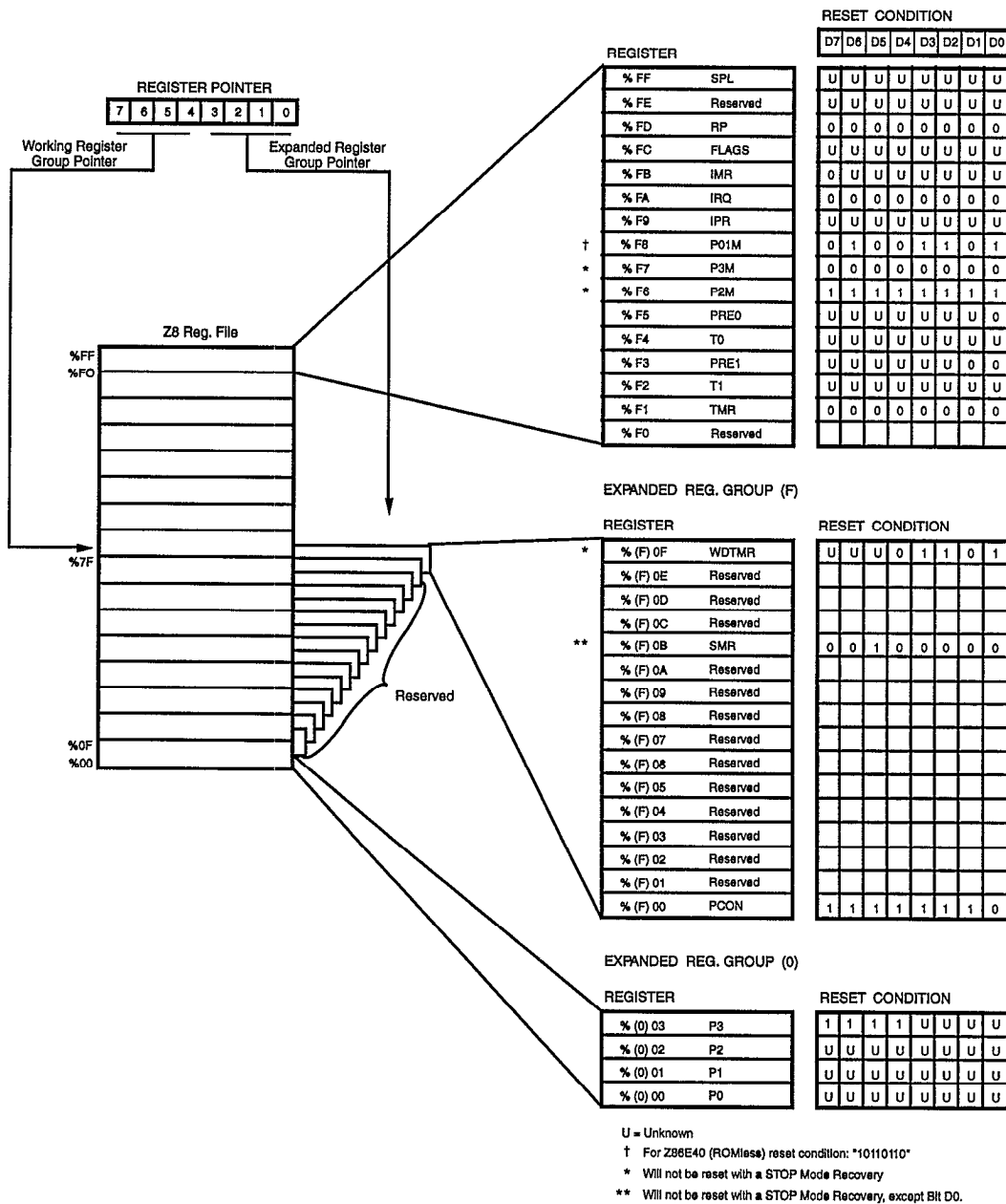


Figure 15. Expanded Register File Architecture

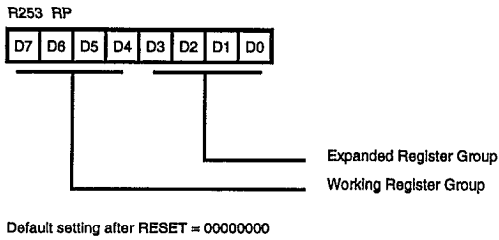
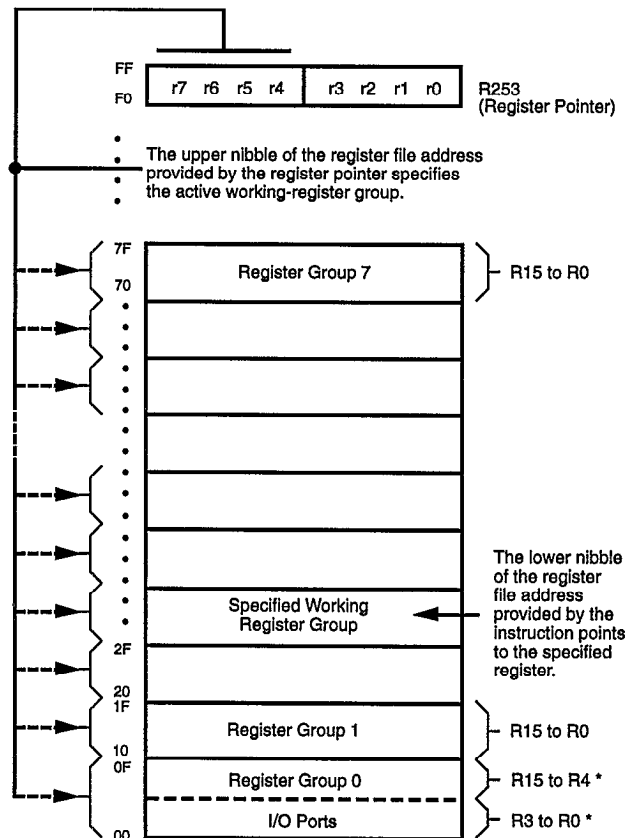


Figure 16. Register Pointer Register

Register File. The 256 byte register file consists of 4 I/O port registers, 236 general-purpose registers and 15 control and status registers (R240 is reserved). The instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addresses using the Register Pointer (Figures 16 and 17). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0H-EFH can only be accessed through working registers and indirect addressing modes.



* Expanded Register Group (0) is selected in this figure by handling bits D3 to D0 as "0" in Register R253 (RP).

Figure 17. Register Pointer

FUNCTIONAL DESCRIPTION (Continued)

GPR. The register R254 is a general-purpose register.

The General Purpose Registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range.

RAM Protect. The upper portion of the RAM's address spaces 80H to EFH (excluding the control registers) can be protected from reading and writing. This option can be selected during the EPROM Programming Mode. After this option is selected, the user can activate this feature from the internal EPROM. D6 of the IMR control register (R251) is used to turn off/on the RAM protect by loading a 0 or 1, respectively. A 1 in D6 indicates RAM Protect enabled.

Stack. The Z86E40 external data memory or the internal register file can be used for the stack. The 16-bit Stack Pointer (R254-R255) is used for the external stack which can reside anywhere in the data memory for ROMless mode, but only from 4096 to 65535 in ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R4-R239). SPH can be used as a general-purpose register when using internal stack only.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by

internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 18).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

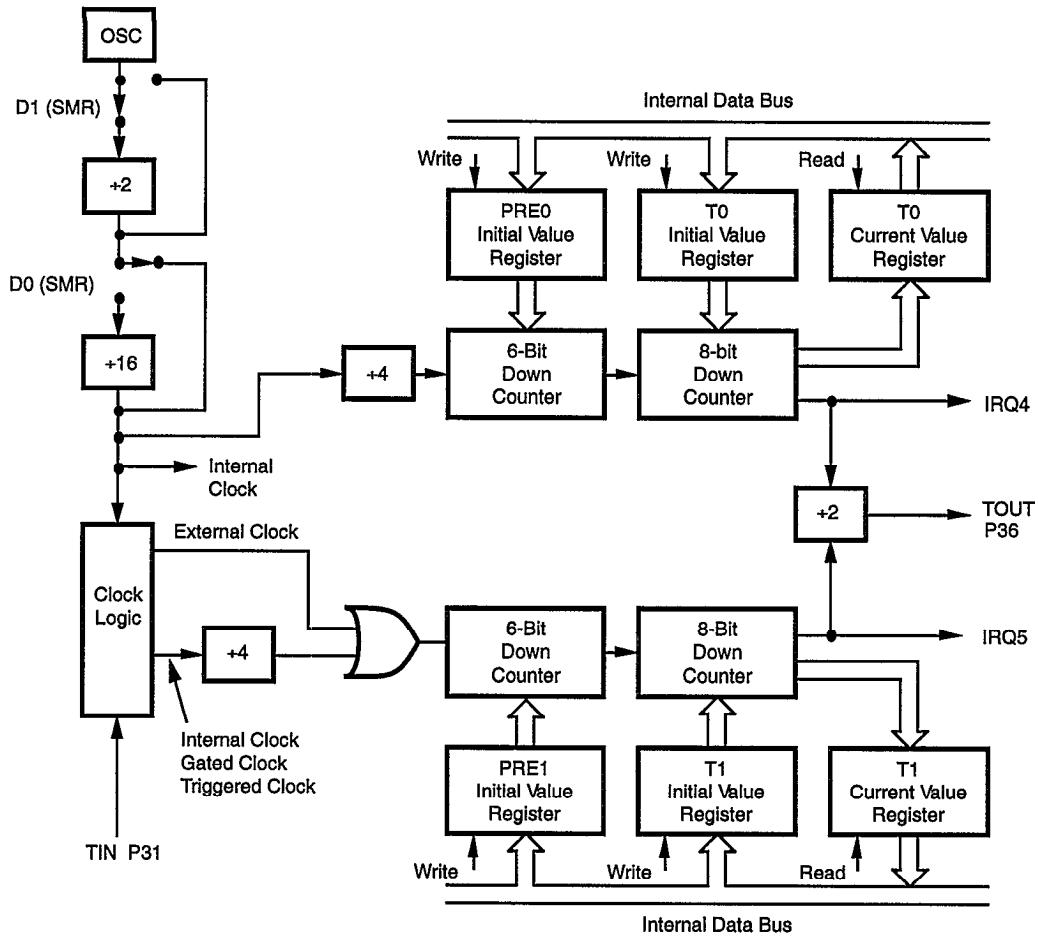


Figure 18. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86E40 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 19). The six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30) and two

in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 8).

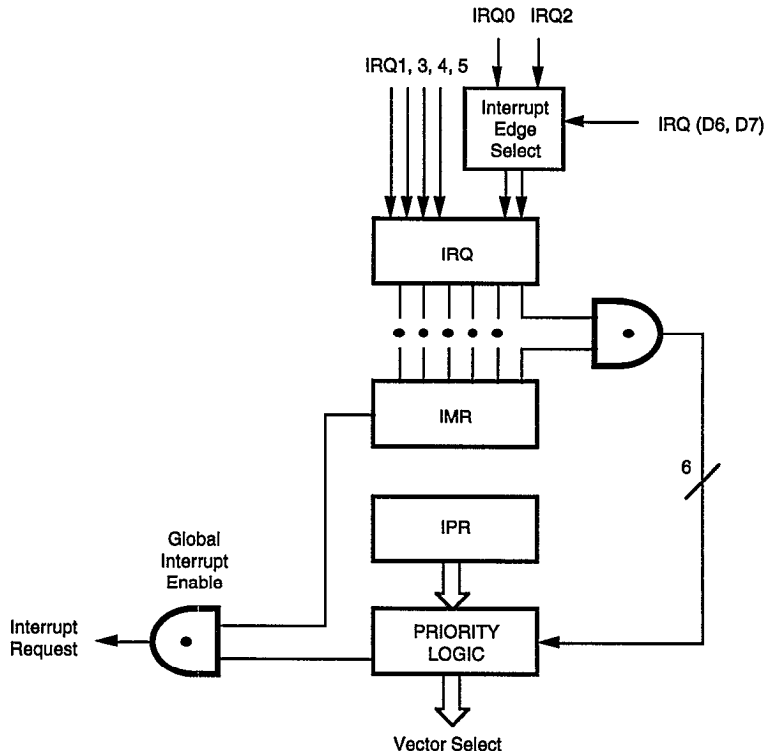


Figure 19. Interrupt Block Diagram

Table 8. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	/DAV2, IRQ2, T _{IN}	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register (IPR). An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86E40 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in bits D7 and D6 of the IRQ Register (R250). The configuration is shown in Table 9.

Table 9. IRQ Register Configuration

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:

F = Falling Edge
R = Rising Edge

Clock. The Z86E40 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitor values from each pin directly to device pin ground. The RC oscillator option can be selected in the programming mode. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 20).

Note: RC OSC does not support 12 MHz.

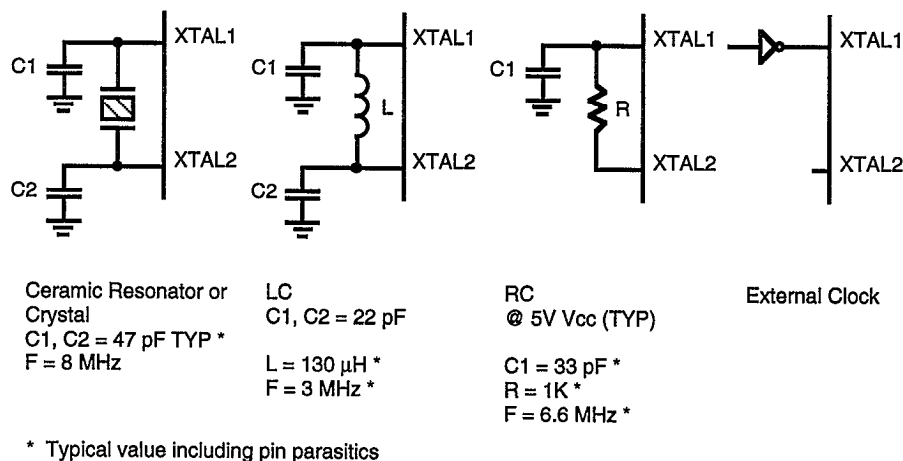


Figure 20. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power fail to Power OK status
2. Stop-Mode Recovery (if D5 of SMR=0)
3. WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP mode Register (SMR) determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for an external clock and RC/LC oscillators with fast start up times).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. STOP mode is terminated by one of the following resets: either by WDT time-out, POR, a Stop-Mode Recovery Source which is defined by the SMR register or external reset. This causes the processor to restart the application program at address 000CH. In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP instruction (opcode=FFH) immediately before the appropriate sleep instruction. For example:

```
FF  NOP ; clear the pipeline
6F  STOP ; enter STOP mode
or
FF  NOP ; clear the pipeline
7F  HALT ; enter HALT mode
```

Port Configuration Register (PCON). The PCON register configures the ports individually; comparator output on Port 3, open-drain on Port 0 and Port 1, low EMI on Ports 0, 1, 2 and 3, and low EMI oscillator. The PCON register is located in the expanded register file at Bank F, location 00 (Figure 21).

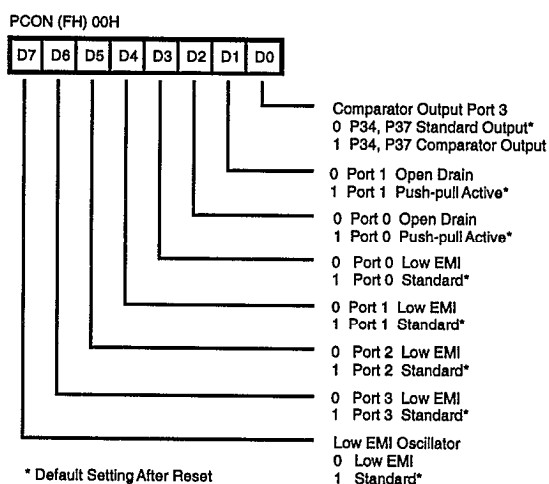


Figure 21. Port Configuration Register (PCON)
(Write Only)

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

Port 1 Open-Drain (D1). Port 1 can be configured as an open-drain by resetting this bit (D1=0) or configured as push-pull active by setting this bit (D1=1). The default value is 1.

Port 0 Open-Drain (D2). Port 0 can be configured as an open-drain by resetting this bit (D2=0) or configured as push-pull active by setting this bit (D2=1). The default value is 1.

Low EMI Port 0 (D3). Port 0 can be configured as a Low EMI Port by resetting this bit (D3=0) or configured as a Standard Port by setting this bit (D3=1). The default value is 1.

Low EMI Port 1 (D4). Port 1 can be configured as a Low EMI Port by resetting this bit (D4=0) or configured as a Standard Port by setting this bit (D4=1). The default value is 1.

Low EMI Port 2 (D5). Port 2 can be configured as a Low EMI Port by resetting this bit (D5=0) or configured as a

Standard Port by setting this bit (D5=1). The default value is 1.

Low EMI Port 3 (D6). Port 3 can be configured as a Low EMI Port by resetting this bit (D6=0) or configured as a Standard Port by setting this bit (D6=1). The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A 1 in this location configures the oscillator with standard drive. While a 0 configures the oscillator with low noise drive, it does not affect the relationship of SCLK and XTAL. The low EMI mode will reduce the drive of the oscillator (OSC). The default value is 1.

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 22). All bits are Write only except Bit 7 which is a Read only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power-on cycle. Bit 6 controls whether a low or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the Stop-Mode Recovery Source. The SMR is located in Bank F of the Expanded Register Group at address OBH.

10

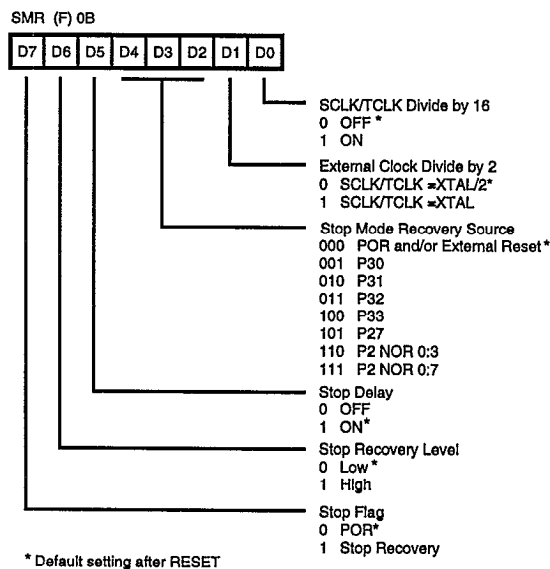


**Figure 22. Stop-Mode Recovery Register
(Write-Only Except Bit D7, Which Is Read-Only)**

FUNCTIONAL DESCRIPTION (Continued)

SCLK/TCLK divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock divide-by-two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, the System Clock (SCLK) and Timer Clock (TCLK) are equal to the external clock frequency divided-by-two. The SCLK/

TCLK is equal to the external clock frequency when this bit is set (D1=1). Using this bit together with D7 of PCON further helps lower EMI (i.e., D7 (PCON) = 0, D1 (SMR) = 1). The default setting is zero.

Stop-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake up source of the Stop-Mode Recovery (Figure 23). Table 10 shows the SMR source selected with the setting of D2 to D4. P33-P31 cannot be used to wake up from STOP mode when programmed as analog inputs.

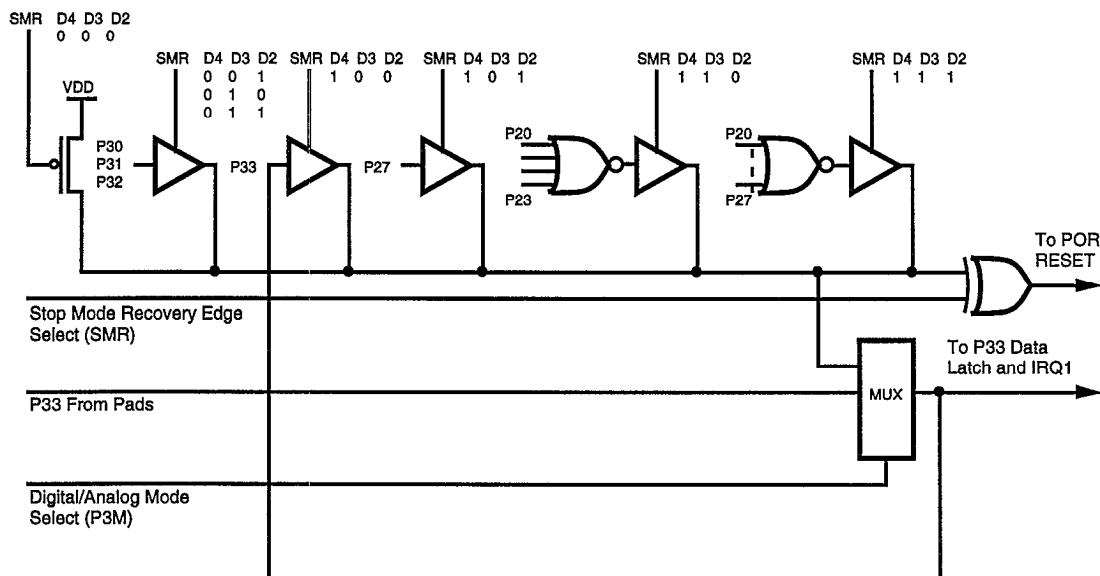


Figure 23. Stop-Mode Recovery Source

Table 10. Stop-Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0-3
1	1	1	Logical NOR of Port 2 bits 0-7

Stop-Mode Recovery Delay Select (D5). The 5 ms RESET delay after Stop-Mode Recovery is disabled by programming this bit to a zero. A 1 in this bit will cause a 5 ms RESET delay after Stop-Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the Stop-Mode Recovery source needs to be kept active for at least 5T_{PC}.

Stop-Mode Recovery Level Select (D6). A 1 in this bit defines that a high level on any one of the recovery sources wakes the Z86E40 from STOP mode. A 0 defines low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. A 0 in this bit indicates that the device has been reset by POR (cold). A 1 in this bit indicates the device was awakened by a SMR source (warm).

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is disabled after Power-On Reset and initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT cannot be disabled when it has been enabled. The WDT is driven either by an on-board RC oscillator or an external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register.

Note: Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.

WDT Timeout Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained (Table 11). The default value of D0 and D1 are 1 and 0, respectively.

Table 11. Timeout Period of the WDT

D1	D0	Timeout of the Internal RC OSC	Timeout of the External Clock
0	0	5 ms	256TpC
0	1	15 ms*	512TpC*
1	0	25 ms	1024TpC
1	1	100 ms	4096TpC

Notes:

TpC = External clock cycle.

The default setting is 15 ms.

WDT During HALT Mode (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates that the WDT is active during HALT. A 0 disables the WDT in HALT mode. The default value is 1.

WDT During STOP Mode (D3). This bit determines whether or not the WDT is active during STOP mode. A 1 indicates active during STOP. A 0 disables the WDT during STOP mode.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator.

Accessibility. The WDTMR register is accessible only during the **first 64** internal system clock cycles from the execution of the first instruction after Power-On Reset, Watch-Dog reset or a Stop-Mode Recovery (Figures 24 and 25). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location OFH.

FUNCTIONAL DESCRIPTION (Continued)

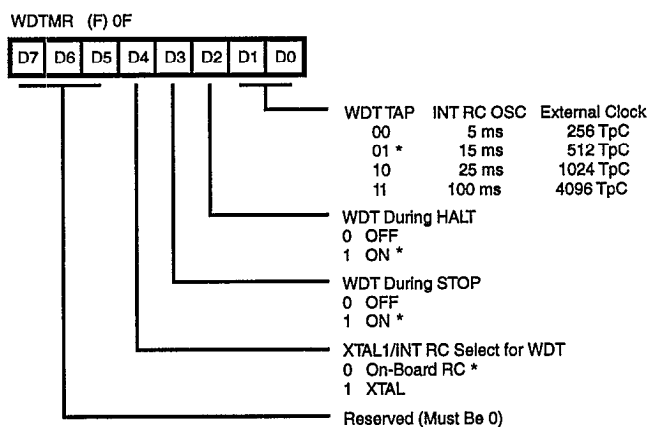


**Figure 24. Watch-Dog Timer Mode Register
(Write Only)**

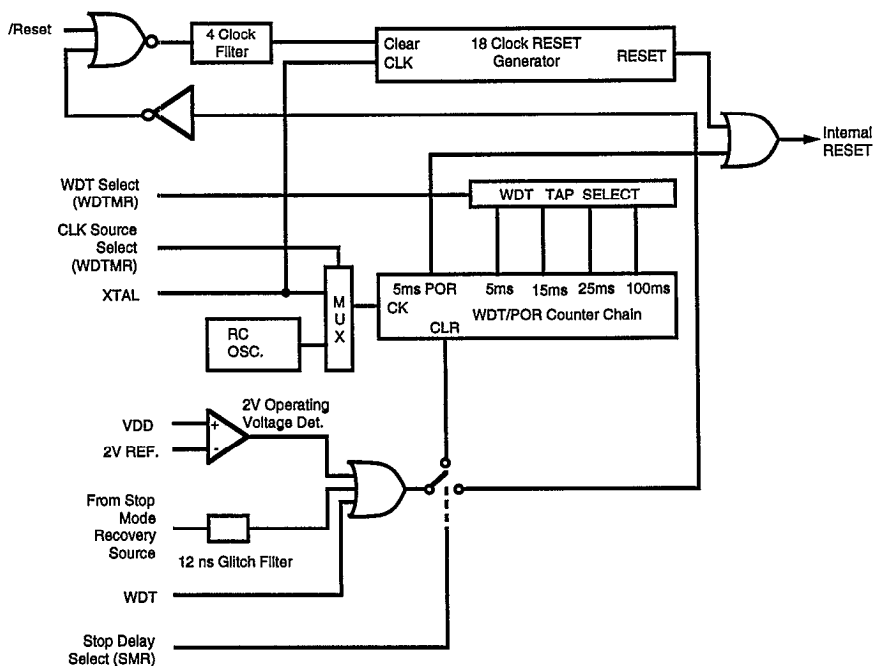


Figure 25. Resets and WDT

Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{RST} (Auto Reset Voltage - Figure 26). If the V_{CC} drops below 4.5V while the device is operating, the device must be powered down, then powered up again.

Note: V_{CC} must be in the allowed operating range (4.5V to 5.5V) prior to the minimum Power-On Reset time-out (T_{POR}).

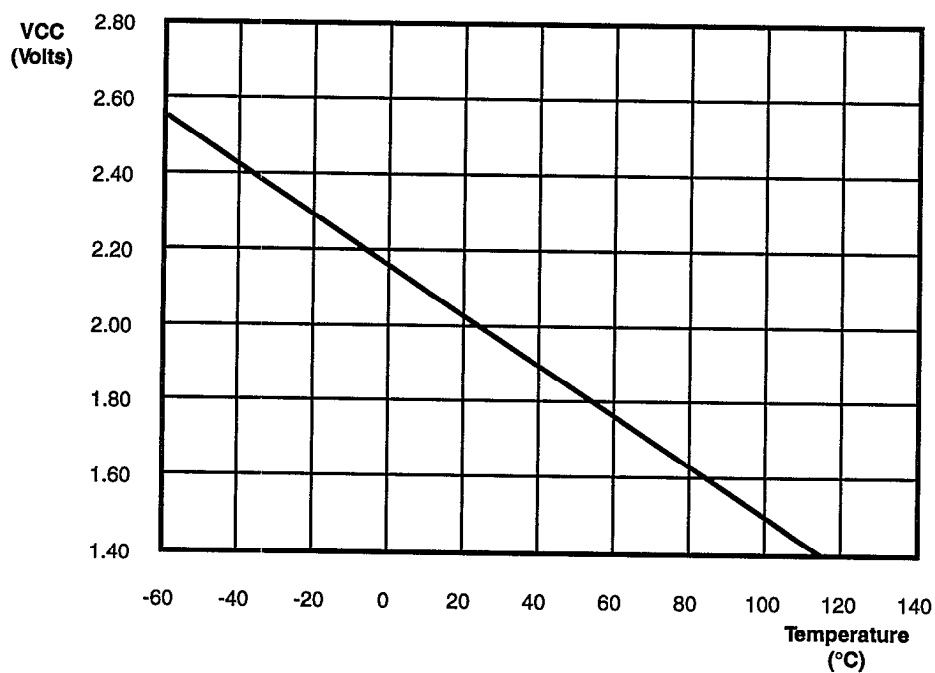


Figure 26. Typical Z86E40 V_{RST} Voltage vs Temperature

FUNCTIONAL DESCRIPTION (Continued)
EPROM Programming Mode

Table 12 shows the programming voltages of each programming mode. Table 13, Figures 27, 28, and 29 show the programming timing of each programming mode. Figure 30 shows the circuit diagram of a Z86E40 programming adaptor, which adapts from 2764A to Z86E40. Figure 31 shows the flow-chart of an Intelligent Programming Algorithm, which is compatible with 2764A EPROM (Z86E40

is 4K EPROM, 2764A is 8K EPROM). Since the EPROM size of Z86E40 differs from 2764A, the programming address range has to be set from 0000H to 0FFFFH. Otherwise, the upper 4K of data (1000H-1FFFFH) will overwrite the lower 4K of data.

Note: EPROM Protect feature disables the LDC, LDCI, LDE, and LDEI instructions, and a ROM look-up table cannot be used with this feature.

Table 12. EPROM Programming Table

Programming Modes	V _{PP}	EPM	/CE	/OE	/PGM	ADDR	DATA	V _{CC} *
EPROM READ1	X	V _H	V _{IL}	V _{IL}	V _{IH}	ADDR	Out	4.5V†
EPROM READ2	V _H	X	V _{IL}	V _{IL}	V _{IH}	ADDR	Out	5.5V†
PROGRAM	V _H	X	V _{IL}	V _{IH}	V _{IL}	ADDR	In	6.0V
PROGRAM VERIFY	V _H	X	V _{IL}	V _{IL}	V _{IH}	ADDR	Out	6.0V
EPROM PROTECT	V _H	V _H	V _H	V _{IH}	V _{IL}	NU	NU	6.0V
RC OSCILLATOR SELECT	V _H	V _{IL}	V _H	V _{IH}	V _{IL}	NU	NU	6.0V
RAM PROTECT	V _H	V _{IH}	V _H	V _{IL}	V _{IL}	NU	NU	6.0V

Notes:

V_H = 12.5V ± 12.5V
V_{IH} = As per specific Z8 DC specification.
V_{IL} = As per specific Z8 DC specification.
X = Not used, but must be set to V_H, V_{IH}, or V_{IL} level.
NU = Not used, but must be set to either V_{IH} or V_{IL} level.

Notes (Continued):

I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
* V_{CC} has a tolerance of ±0.25V.
† Although most programmers do an EPROM read at V_{CC} = 5.0, Zilog recommends an EPROM read at V_{CC} = 4.5 and 5.0 to ensure proper device operations during the V_{CC} after programming.

Table 13. EPROM Programming Timing

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		μs
2	Data Setup Time	2		μs
3	V _{PP} Setup	2		μs
4	V _{CC} Setup Time	2		μs
5	Chip Enable Setup Time	2		μs
6	Program Pulse Width	0.95	1.05	ms
7	Data Hold Time	2		μs
8	/OE Setup Time	2		μs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		μs
13	/PGM Setup Time	2		μs
14	Address to /OE Setup Time	2		μs
15	Option Program Pulse Width	78		ms

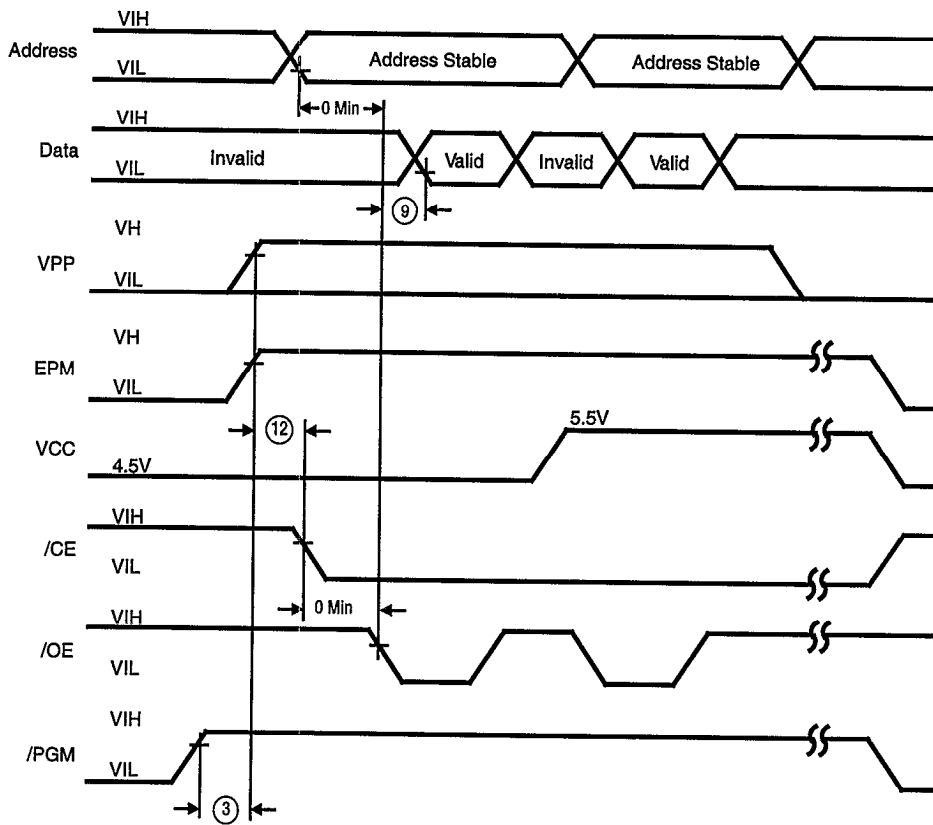


Figure 27. EPROM READ Mode Timing Diagram

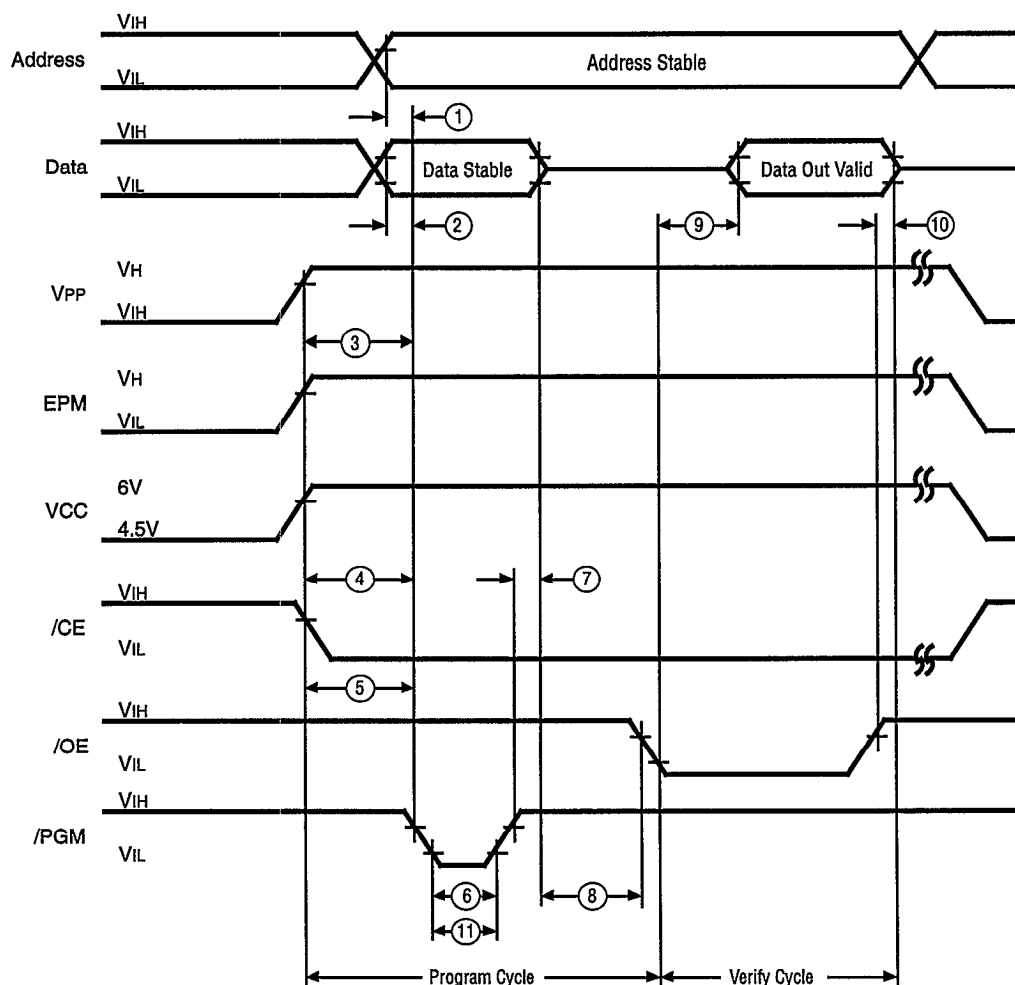
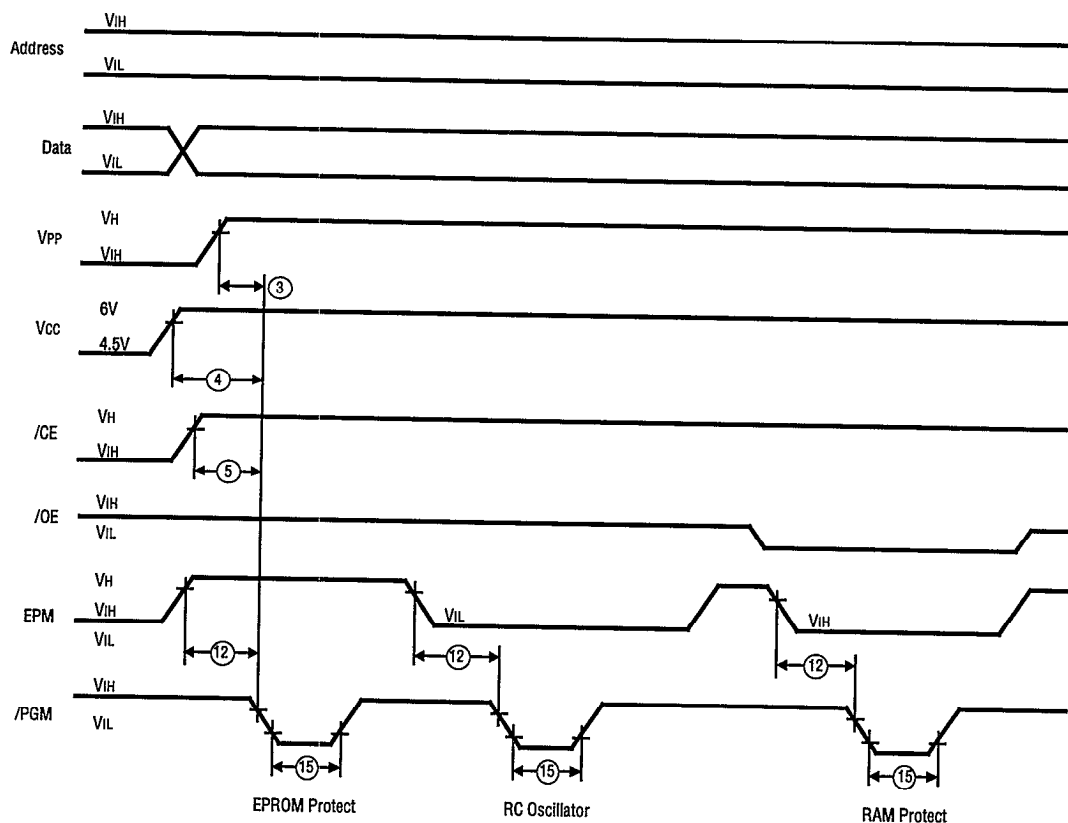
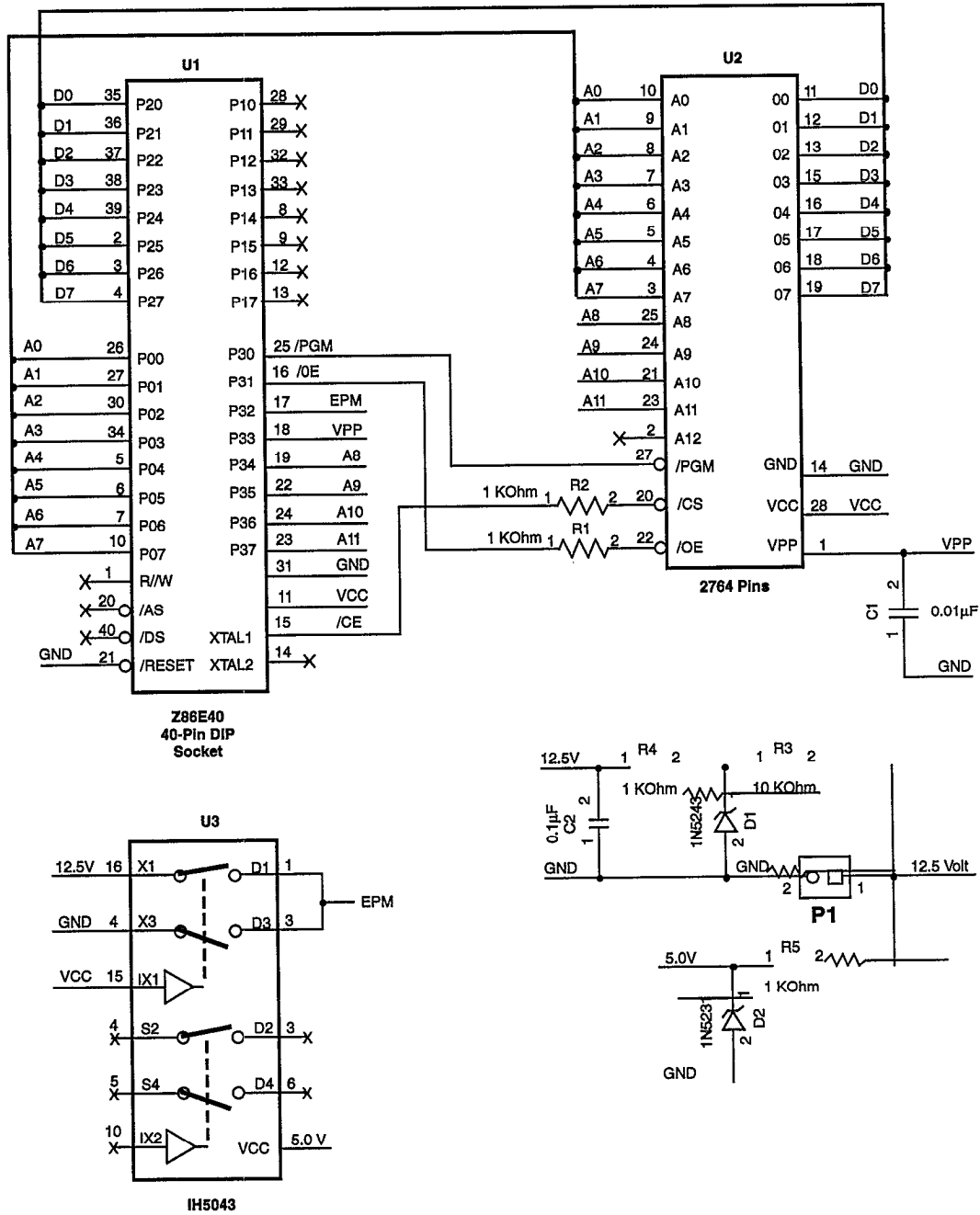
Z86E40 TIMING DIAGRAMS


Figure 28. Timing Diagram of EPROM Program and Verify Modes



10

Figure 29. Timing Diagram of EPROM Protect, RAM Protect and RC OSC Modes

FUNCTIONAL DESCRIPTION (Continued)

Figure 30. Z86E40 Z8 OTP Programming Adapter

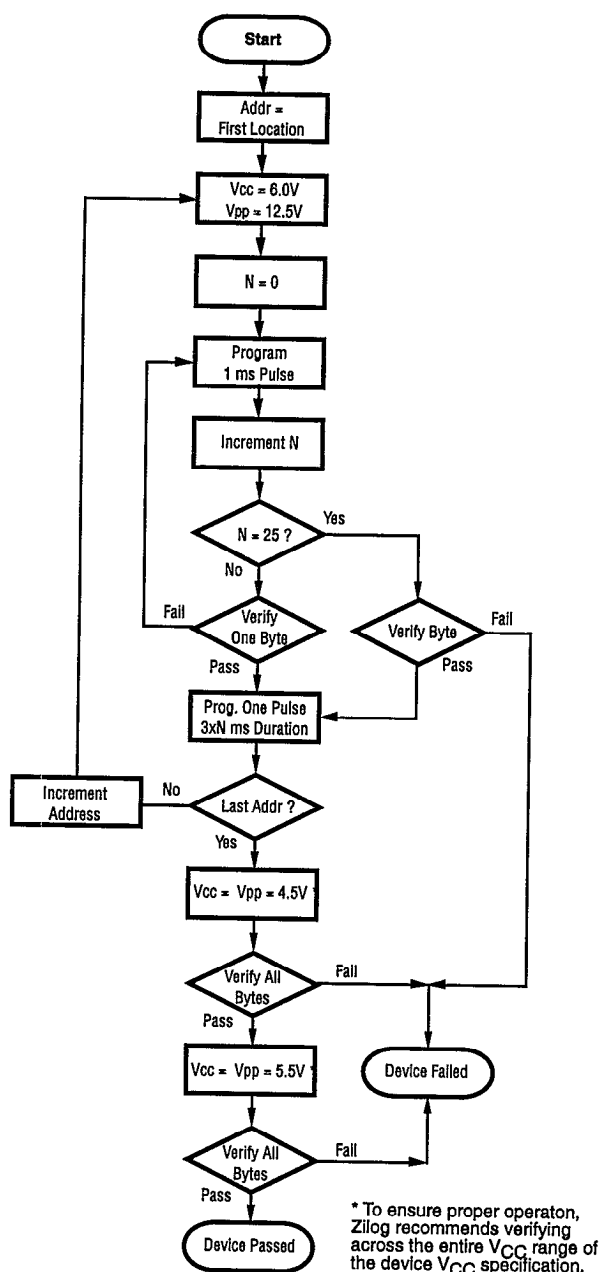


Figure 31. Z86E40 Programming Algorithm

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	-0.3	+7.0	V
T_{STG}	Storage Temp	-65°	+150°	C
T_A	Oper Ambient Temp	†	†	C
	Power Dissipation		2.2	W

Notes:

* Voltage on all pins with respect to GND.

† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 32).

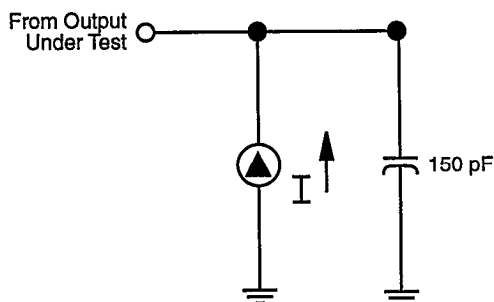


Figure 32. Test Load Diagram

CAPACITANCE

$T_A = 25^\circ\text{C}$; $V_{CC} = \text{GND} = 0\text{V}$; $f = 1.0\text{ MHz}$; unmeasured pins to GND.

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

V_{CC} SPECIFICATION

$V_{CC} \quad 5.0\text{V} \pm 0.5\text{V}$

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC} Note[3]	T _A = 0°C to +70°C		Typical at 25°C	Units	Conditions	Notes
			Min	Max				
	Max Input Voltage	5.0V		V _{CC} + 0.5V		V	I _{IN} < 250 µA	[7]
V _{CH}	Clock Input High Voltage	5.0V	0.7 V _{CC}	V _{CC} + 0.3V	2.5	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	5.0V	V _{SS} - 0.3	0.2 V _{CC}	1.5	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	5.0V	0.7 V _{CC}	V _{CC} + 0.3	2.5	V		[7]
V _{IL}	Input Low Voltage	5.0V	V _{SS} - 0.3	0.2 V _{CC}	1.5	V		
V _{OH}	Output High Voltage (Low EMI Mode)	5.0V	V _{CC} - 0.4		4.8	V	I _{OH} = -2.0 mA	[9]
		5.0V	V _{CC} - 0.4			V	I _{OH} = -0.5 mA	[8]
V _{OL1}	Output Low Voltage (Low EMI Mode)	5.0V		0.4	0.1	V	I _{OL} = +4.0 mA	[9]
		5.0V		0.4	0.1	V	I _{OL} = +1.0 mA	[8]
V _{OL2}	Output Low Voltage	5.0V		1.5	0.3	V	I _{OL} = +12 mA, 3 Pin Max	[9]
V _{RH}	Reset Input High Voltage	5.0V	0.7 V _{CC}	V _{CC} + 0.3	2.1	V		
V _{RI}	Reset Input Low Voltage	5.0V	V _{SS} - 0.3	0.2 V _{CC}	1.7	V		
V _{OFFSET}	Comparator Input Offset Voltage	5.0V		50	10	mV		
I _{IL}	Input Leakage	5.0V	-10	+10	< 1	µA	V _{IN} = 0V, V _{CC}	
I _{OL}	Output Leakage	5.0V	-10	+10	< 1	µA	V _{IN} = 0V, V _{RL} = 0	
I _{IR}	Reset Input Current	5.0V		60	45	µA	V _{CC} = 5.0V,	
I _{CC}	Supply Current (Standard Mode)	5.0V		16	15.0	mA	Ⓢ 8 MHz	[4,5]
				20	18	mA	Ⓢ 12 MHz	[4,5]

10

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V _{CC} Note[3]	T _A = 0°C to +70°C		Typical at 25°C	Units	Conditions	Notes
			Min	Max				
I _{CC1}	Standby Current (Standard Mode)	5.0V		6.0	3.5	mA	HALT mode V _{IN} = 0V, V _{CC} ⊗ 8 MHz	[4,5]
		5.0V		7.5	4.5	mA	HALT mode V _{IN} = 0V, V _{CC} ⊗ 12 MHz	[4,5]
		5.0V		3.0	1.5	mA	Clock Divide by 16 ⊗ 8 MHz	[4,5]
		5.0V		3.0	1.7	mA	Clock Divide by 16 ⊗ 12 MHz	[4,5]
I _{CC}	Supply Current (Low EMI Mode)	5.0V		7.5	5.0	mA	⊗ 2 MHz	[4,5]
		5.0V		12.0	8.0	mA	⊗ 4 MHz	[4,5]
I _{CC1}	Standby Current (Low EMI Mode)	5.0V		2.0	1.0	mA	⊗ 2 MHz	[4,5]
		5.0V		3.0	1.5	mA	⊗ 4 MHz	[4,5]
		5.0V		2.0	0.75	mA	Clock Divide-by-16 ⊗ 2 MHz	[4,5]
		5.0V		2.0	1.0	mA	Clock Divide-by-16 ⊗ 4 MHz	[4,5]
I _{CC2}	Standby Current	5.0V		10	2	μA	STOP mode V _{IN} = 0V, V _{CC} WDT is not Running	[6]
		5.0V		800	450	μA	STOP mode V _{IN} = 0V, V _{CC} WDT is Running	[6,10]
I _{ALL}	Auto Latch Low Current	5.0V		-10	-5	μA	0V < V _{IN} < V _{CC}	
I _{ALH}	Auto Latch High Current	5.0V		20	10	μA	0V < V _{IN} < V _{CC}	
T _{POR}	Power-On Reset	5.0V		2.5	4.5	ms		
V _{RST}	Auto Reset Voltage				2.6	V		

Notes:

- [1] I_{CC1}
- | | | | |
|--------|-----|------|-------|
| Typ | Max | Unit | Freq |
| 0.3 mA | 6.0 | mA | 8 MHz |
| 3.5 mA | 6.0 | mA | 8 MHz |
- Clock-driven crystal or resonator
- [2] V_{SS}=0V=GND.
- [3] V_{CC} must be in the allowed operating range (4.5V to 5.5V) prior to the minimum T_{POR} timeout. V_{CC} specified at 4.5V to 5.5V.
- [4] All outputs unloaded, I/O pins floating, inputs at rail.
- [5] CL1=CL2=100 pF.
- [6] Same as note [4] except inputs at V_{CC}.
- [7] Except clock pins and Port 3 input pins in EPROM mode.
- [8] Port Low EMI mode.
- [9] Port STD mode.
- [10] Internal RC

AC ELECTRICAL CHARACTERISTICS

External I/O or Memory Read/Write Timing Diagrams (Standard Mode)

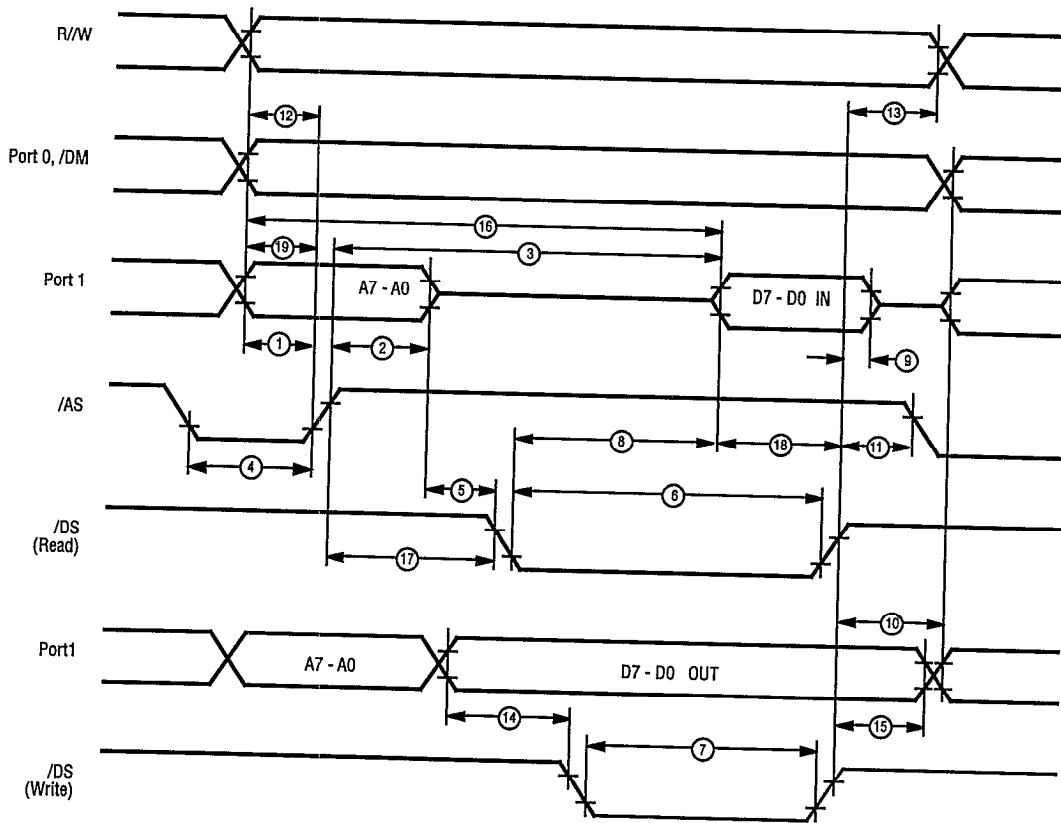


Figure 33. External I/O or Memory Read/Write Timing

AC ELECTRICAL CHARACTERISTICS

External I/O or Memory Read/Write Timing (Standard Mode)

Standard Mode									
No	Sym	Parameter	V _{CC} Note [1]	8 MHz Min	8 MHz Max	12 MHz Min	12 MHz Max	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	5.0V	35		35		ns	[2]
2	TdAS(A)	/AS Rise to Address Float Delay	5.0V	70		45		ns	[2]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid	5.0V		400		250	ns	[1,2]
4	TwAS	/AS Low Width	5.0V	80		55		ns	[2]
5	TdAS(DS)	Address Float to /DS Fall	5.0V	0		0		ns	
6	TwDSR	/DS (Read) Low Width	5.0V	300		200		ns	[1,2]
7	TwDSW	/DS (Write) Low Width	5.0V	165		110		ns	[1,2]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid	5.0V		260		160	ns	[1,2]
9	ThDR(DS)	Read Data /DS Rise Hold Time	5.0V	0		0		ns	[2]
10	TdDS(A)	/DS Rise to Address Active Delay	5.0V	95		55		ns	[2]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	5.0V	70		45		ns	[2]
12	TdR/W(AS)	R/W Valid to /AS Rise Delay	5.0V	70		45		ns	[2]
13	TdDS(R/W)	/DS Rise to R/W Not Valid	5.0V	70		45		ns	[2]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	5.0V	80		55		ns	[2]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	5.0V	80		55		ns	[2]
16	TdA(DR)	Address Valid to Read Data Req'd Valid	5.0V		475		310	ns	[1,2]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	5.0V	100		65		ns	[2]
18	TdDI(DS)	Data Output Setup to /DS Rise	5.0V	75		75		ns	[1,2]
19	TdDM(AS)	/DM Valid to /AS Fall Delay	5.0V	55		35		ns	[2]

Notes:

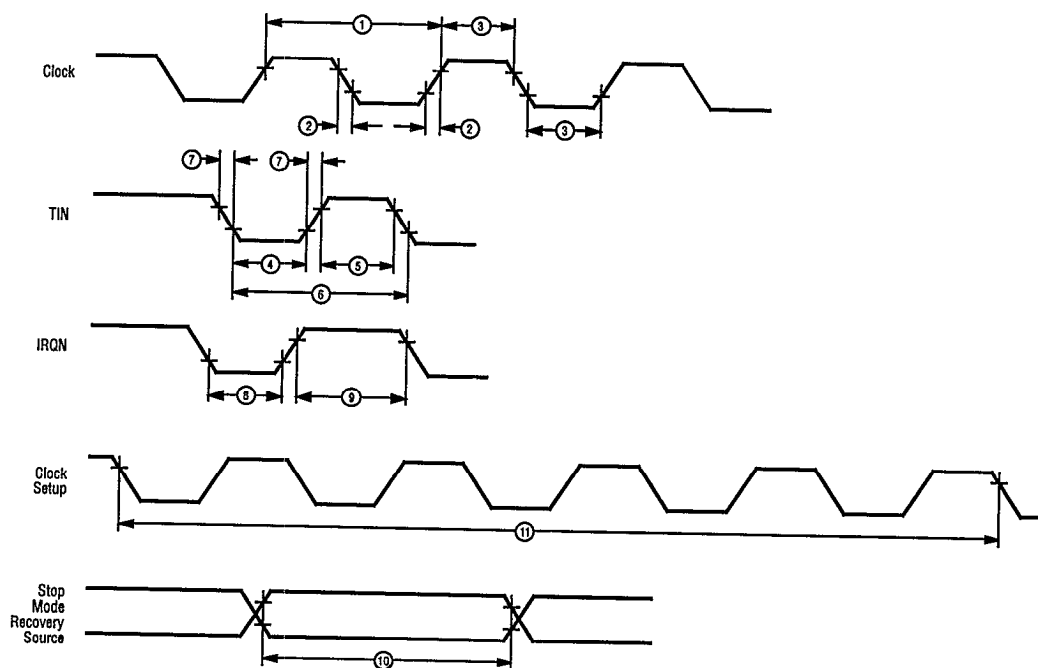
[1] When using extended memory timing add 2TpC.

[2] Timing numbers given are for minimum TpC.

 [3] 5.0V ±0.5V Standard Test Load. All timing references use 0.7V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0. Standard operating temperature range 0°C to +70°C.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagrams (Standard Mode)



10

Figure 34. Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table (Standard Mode)

No	Sym	Parameter	V _{cc} Note [3]	Standard Mode		Units	Notes		
				8 MHz	12 MHz				
			Min	Max	Min	Max			
1	TpC	Input Clock Period	5.0V	125	DC	83	DC	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times	5.0V		25		15	ns	[1]
3	TwC	Input Clock Width	5.0V	62.5		41.5		ns	[1]
4	TwTinL	Timer Input Low Width	5.0V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	5.0V	5TpC		5TpC			[1]
6	TpTin	Timer Input Period	5.0V	8TpC		8TpC			[1]
7	TrTin,TfTin	Timer Input Rise & Fall Timers	5.0V		100		100	ns	[1]
8A	TwIL	Int. Request Low Time	5.0V	70		70		ns	[1,2]
8B	TwIL	Int. Request Low Time	5.0V	5TpC		5TpC			[1,3]
9	TwIH	Int. Request Input High Time	5.0V	5TpC		5TpC			[1,2]
10	Twsm	Stop-Mode Recovery Width Spec	5.0V	12		12		ns	[11]
			5.0V	5TpC		5TpC			[10]
11	Tost	Oscillator Startup Time	5.0V		5TpC		5TpC		[4]
12	Twdt	Watch-DogTimer Delay Time	5.0V	5		5		ms	[6]
			5.0V	15		15		ms	[7]
			5.0V	25		25		ms	[8]
			5.0V	100		100		ms	[9]

Notes:

[1] Timing Reference uses 0.7 V_{cc} for a logic 1 and 0.2 V_{cc} for a logic 0.

[2] Interrupt request through Port 3 (P33-P31).

[3] Interrupt request through Port 3 (P30)

[4] SMR-D5 = 0

[5] 5.0V ±0.5V

[6] Reg. WDTMR D1=0, D0=0

[7] Reg. WDTMR D1=0, D0=1

[8] Reg. WDTMR D1=1, D0=0

[9] Reg. WDTMR D1=1, D0=1

[10] Reg. SMR-D5=0. No Delay

[11] Reg. SMR-D5=1. With Delay

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Diagrams

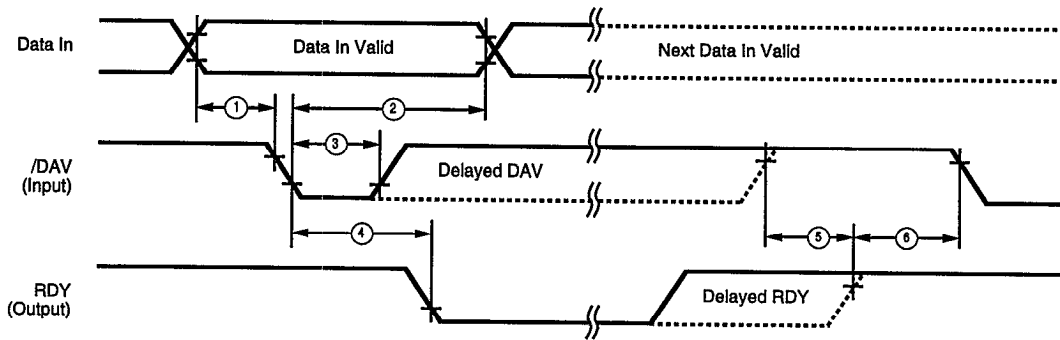


Figure 34. Input Handshake Timing

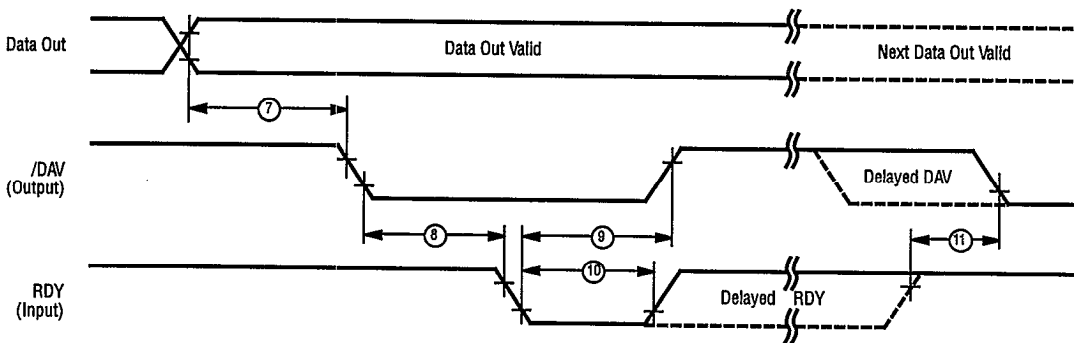


Figure 35. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table - (Standard Modes)

No	Sym	Parameter	V _{cc} Note[1]	Standard Mode				Data Direction
				8 MHz		12 MHz		
				Min	Max	Min	Max	
1	TsDI(DAV)	Data In Setup Time	5.0V	0		0		IN
2	ThDI(DAV)	Data In Hold Time	5.0V	115		115		IN
3	TwDAV	Data Available Width	5.0V	110		110		IN
4	TdDAV(RDY)	DAV Fall to RDY Fall Delay	5.0V		115		115	IN
5	TdDAVd(RDY)	DAV Rise to RDY Rise Delay	5.0V		80		80	IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	5.0V	0		0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay	5.0V	63		42		OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	5.0V	0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	5.0V		115		115	OUT
10	TwRDY	RDY Width	5.0V	80		80		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	5.0V		80		80	OUT

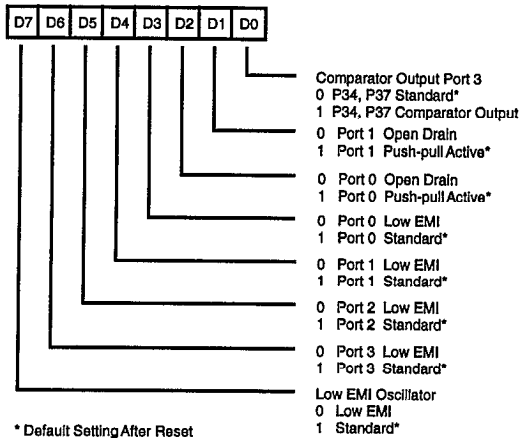
Notes:

[1] 5.0 V ±0.5V

Standard operating temperature range 0°C to +70°C

EXPANDED REGISTER FILE CONTROL REGISTERS

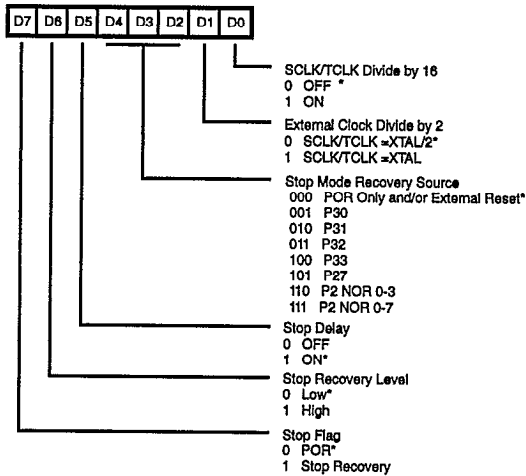
PCON (FH) 00H



* Default Setting After Reset

**Figure 36. Port Configuration Register
(Write Only)**

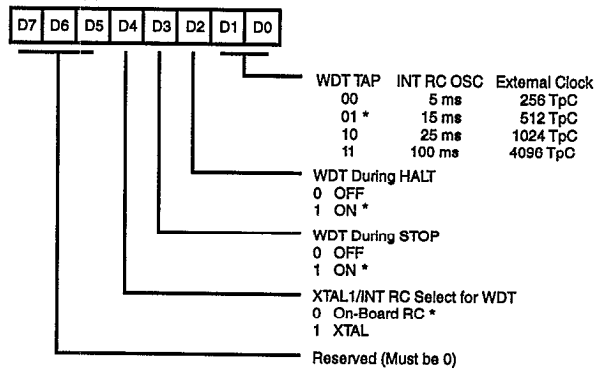
SMR (FH) 0B



* Default setting after RESET

**Figure 37. Stop-Mode Recovery Register
(Write Only Except Bit D7, Which is Read Only)**

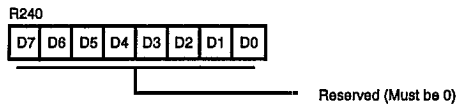
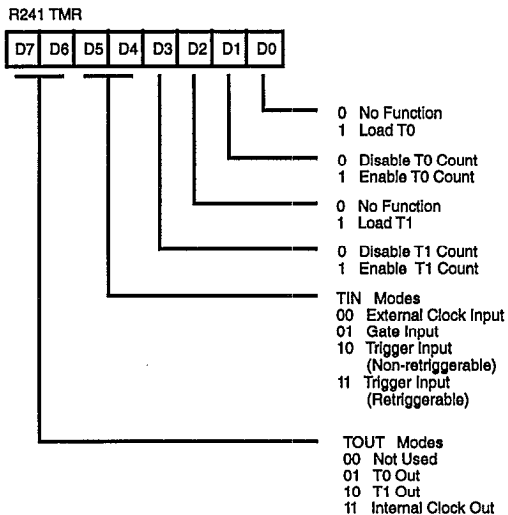
WDTMR (F) 0F



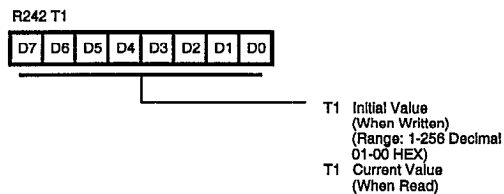
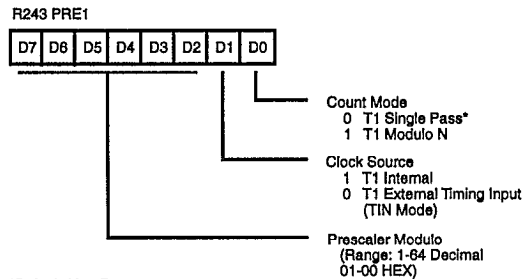
* Default setting after RESET

**Figure 38. Watch-Dog Timer Mode Register
(Write Only)**

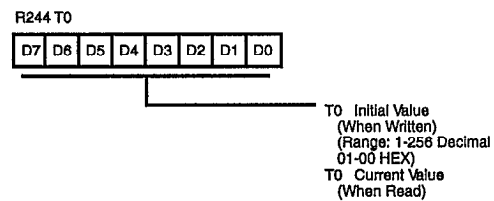
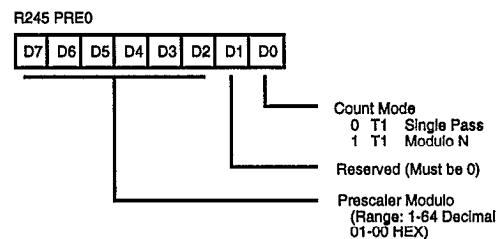
10

Z8 CONTROL REGISTER DIAGRAMS

Figure 39. Reserved


Default After Reset = 00H

Figure 40. Timer Mode Register (F1H: Read/Write)

Figure 41. Counter/Timer 1 Register (F2H: Read/Write)


*Default After Reset

Figure 42. Prescaler 1 Register (F3H: Write Only)

Figure 43. Counter/Timer 0 Register (F4H: Read/Write)

Figure 44. Prescaler 0 Register (F5H: Write Only)

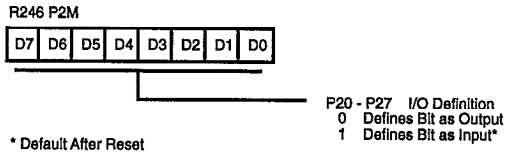


Figure 45. Port 2 Mode Register (F6H: Write Only)

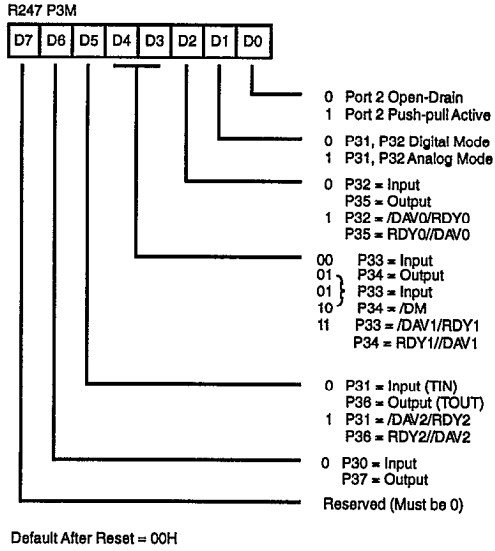


Figure 46. Port 3 Mode Register (F7H: Write Only)

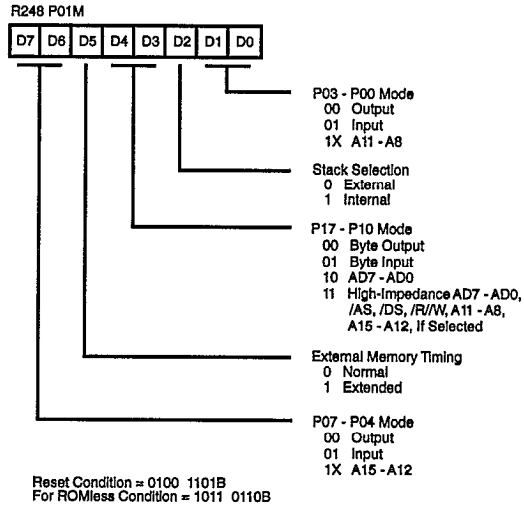


Figure 47. Port 0 and 1 Mode Register (F8H: Write Only)

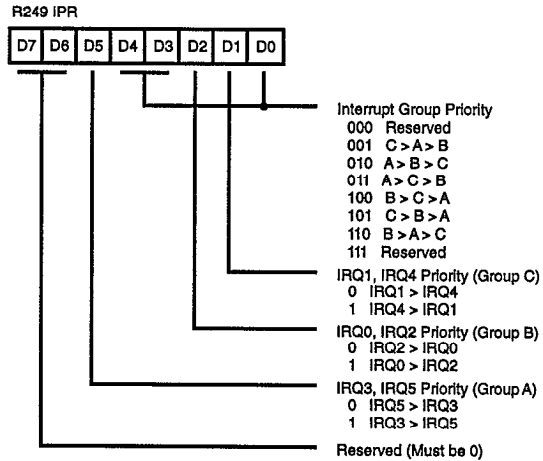


Figure 48. Interrupt Priority Register (F9H: Write Only)

10

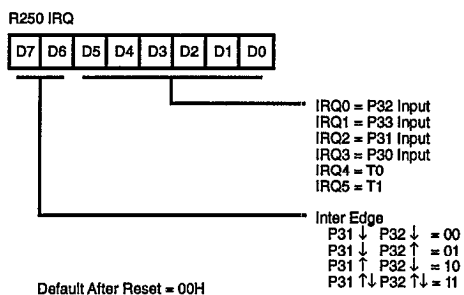
Z8 CONTROL REGISTER DIAGRAMS (Continued)


Figure 49. Interrupt Request Register
(FAH: Read/Write)

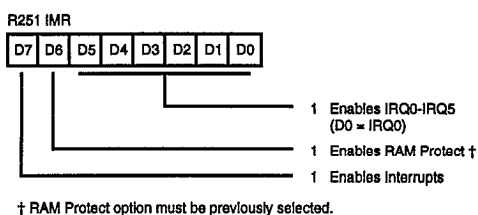


Figure 50. Interrupt Mask Register
(FBH: Read/Write)

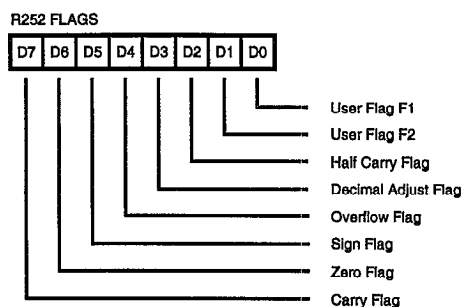


Figure 51. Flag Register
(FCH: Read/Write)

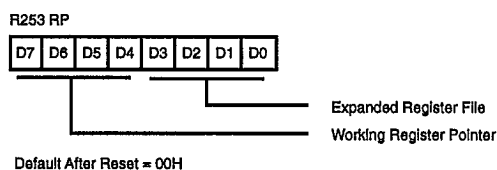


Figure 52. Register Pointer
(FDH: Read/Write)

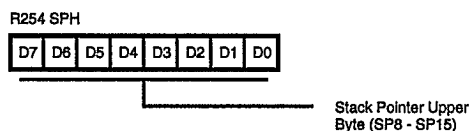


Figure 53. Stack Pointer High
(FEH: Read/Write)

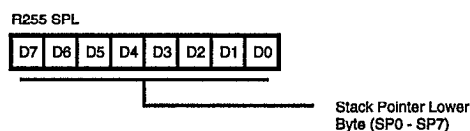


Figure 54. Stack Pointer Low
(FFH: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

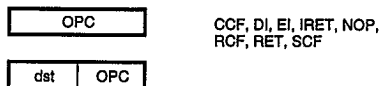
Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
–	Unaffected
x	Undefined

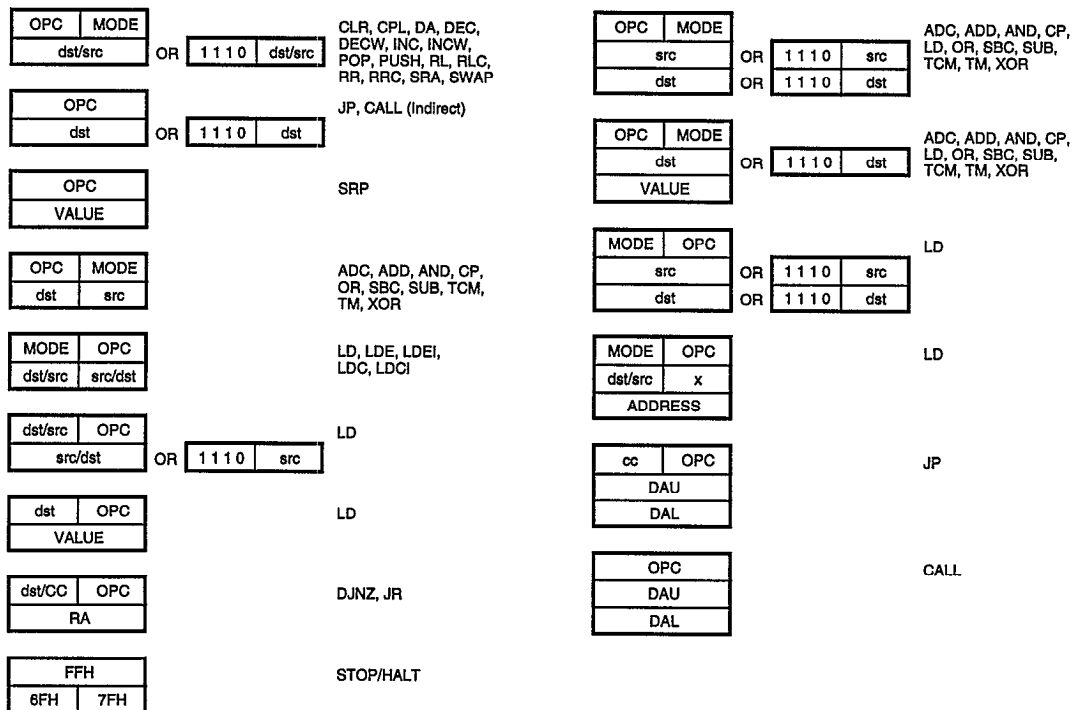
CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	—
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	—

INSTRUCTION FORMATS



One-Byte Instructions



10

Two-Byte Instructions

Three-Byte Instructions

INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " $\leftarrow$ ". For example:

$$\text{dst} \leftarrow \text{dst} + \text{src}$$

Indicates that the source data is added to the destination data and the result is stored in the destination location. The

notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

$$\text{dst} (7)$$

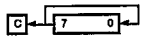
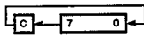
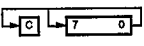
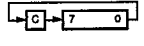
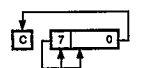
refers to bit 7 of the destination operand.

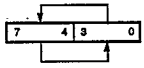
INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected						
			C	Z	S	V	D	H	
ADC dst, src dst ← dst + src + C	†	1[]	*	*	*	*	0	*	
ADD dst, src dst ← dst + src	†	0[]	*	*	*	*	0	*	
AND dst, src dst ← dst AND src	†	5[]	-	*	*	*	0	-	-
CALL dst SP ← SP - 2 @SP ← PC, PC ← dst	DA IRR	D6 D4	-	-	-	-	-	-	-
CCF C ← NOT C		EF	*	-	-	-	-	-	-
CLR dst dst ← 0	R IR	B0 B1	-	-	-	-	-	-	-
COM dst dst ← NOT dst	R IR	60 61	-	*	*	*	0	-	-
CP dst, src dst - src	†	A[]	*	*	*	*	-	-	-
DA dst dst ← DA dst	R IR	40 41	*	*	*	*	X	-	-
DEC dst dst ← dst - 1	R IR	00 01	-	*	*	*	*	-	-
DECW dst dst ← dst - 1	RR IR	80 81	-	*	*	*	*	-	-
DI IMR(7) ← 0		8F	-	-	-	-	-	-	-
DJNZ r, dst r ← r - 1 if r ≠ 0 PC ← PC + dst Range: +127, -128	RA	rA r = 0 - F	-	-	-	-	-	-	-
EI IMR(7) ← 1		9F	-	-	-	-	-	-	-
HALT		7F	-	-	-	-	-	-	-

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected						
			C	Z	S	V	D	H	
INC dst dst ← dst + 1	r R IR	rE r = 0 - F 20 21	-	*	*	*	*	-	-
INCW dst dst ← dst + 1	RR IR	A0 A1	-	*	*	*	*	-	-
IRET FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR(7) ← 1		BF	*	*	*	*	*	*	*
JP cc, dst if cc is true, PC ← dst	DA IRR	cD c = 0 - F 30	-	-	-	-	-	-	-
JR cc, dst if cc is true, PC ← PC + dst Range: +127, -128	RA	cB c = 0 - F	-	-	-	-	-	-	-
LD dst, src dst ← src	r Im r R R r r X X r r Ir Ir r R R R IR R IM IR IM IR R	rC r8 r9 r = 0 - F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-	-
LDC dst, src dst ← src	r lrr	C2	-	-	-	-	-	-	-
LDCI dst, src dst ← src r ← r + 1; r ← r + 1	lr lrr	C3	-	-	-	-	-	-	-
NOP		FF	-	-	-	-	-	-	-

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected				
			C	Z	S	V	D H
OR dst, src dst ← dst OR src	†	4[]	-	*	*	0	- -
POP dst dst ← @SP; SP ← SP + 1	R IR	50 51	-	-	-	-	- -
PUSH src SP ← SP - 1; @SP ← src	R IR	70 71	-	-	-	-	- -
RCF C ← 0		CF	0	-	-	-	- -
RET PC ← @SP; SP ← SP + 2		AF	-	-	-	-	- -
RL dst 	R IR	90 91	*	*	*	*	- -
RLC dst 	R IR	10 11	*	*	*	*	- -
RR dst 	R IR	E0 E1	*	*	*	*	- -
RRC dst 	R IR	C0 C1	*	*	*	*	- -
SBC dst, src dst ← dst - src - C	†	3[]	*	*	*	*	1 *
SCF C ← 1		DF	1	-	-	-	- -
SRA dst 	R IR	D0 D1	*	*	*	0	- -
SRP dst RP ← src	Im	31	-	-	-	-	- -

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected				
			C	Z	S	V	D H
STOP		6F	1	-	-	-	- -
SUB dst, src dst ← dst - src	†	2[]	*	*	*	*	1 *
SWAP dst 	R IR	F0 F1	X	*	*	X	- -
TCM dst, src (NOT dst) AND src	†	6[]	-	*	*	0	- -
TM dst, src dst AND src	†	7[]	-	*	*	0	- -
XOR dst, src ds ← dst XOR src	†	B[]	-	*	*	0	- -
WDT		5F	-	X	X	X	- -

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

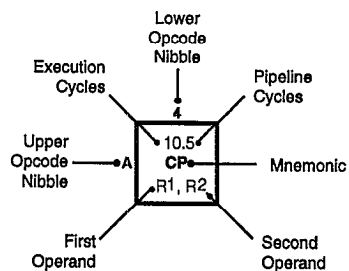
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst src		Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

10

OPCODE MAP

		Lower Nibble (Hex)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Upper Nibble (Hex)	0	6.5 DEC R1	6.5 DEC IR1	6.5 ADD r1, r2	6.5 ADD r1, Ir2	10.5 ADD R2, R1	10.5 ADD IR2, R1	10.5 ADD R1, IM	10.5 ADD IR1, IM	6.5 LD r1, R2	6.5 LD r2, R1	12/10.5 DJNZ r1, RA	12/10.0 JR cc, RA	6.5 LD r1, IM	12.10.0 JP cc, DA	6.5 INC r1	
	1	6.5 RLC R1	6.5 RLC IR1	6.5 ADC r1, r2	6.5 ADC r1, Ir2	10.5 ADC R2, R1	10.5 ADC IR2, R1	10.5 ADC R1, IM	10.5 ADC IR1, IM								
	2	6.5 INC R1	6.5 INC IR1	6.5 SUB r1, r2	6.5 SUB r1, Ir2	10.5 SUB R2, R1	10.5 SUB IR2, R1	10.5 SUB R1, IM	10.5 SUB IR1, IM								
	3	8.0 JP IRR1	6.1 SRP IM	6.5 SBC r1, r2	6.5 SBC r1, Ir2	10.5 SBC R2, R1	10.5 SBC IR2, R1	10.5 SBC R1, IM	10.5 SBC IR1, IM								
	4	8.5 DA R1	8.5 DA IR1	6.5 OR r1, r2	6.5 OR r1, Ir2	10.5 OR R2, R1	10.5 OR IR2, R1	10.5 OR R1, IM	10.5 OR IR1, IM								
	5	10.5 POP R1	10.5 POP IR1	6.5 AND r1, r2	6.5 AND r1, Ir2	10.5 AND R2, R1	10.5 AND IR2, R1	10.5 AND R1, IM	10.5 AND IR1, IM								6.0 WDT
	6	6.5 COM R1	6.5 COM IR1	6.5 TCM r1, r2	6.5 TCM r1, Ir2	10.5 TCM R2, R1	10.5 TCM IR2, R1	10.5 TCM R1, IM	10.5 TCM IR1, IM								6.0 STOP
	7	10/12.1 PUSH R2	12/14.1 PUSH IR2	6.5 TM r1, r2	6.5 TM r1, Ir2	10.5 TM R2, R1	10.5 TM IR2, R1	10.5 TM R1, IM	10.5 TM IR1, IM								7.0 HALT
	8	10.5 DECW RR1	10.5 DECW IR1	12.0 LDE r1, Ir2	18.0 LDEI Ir1, Ir2												6.1 DI
	9	6.5 RL R1	6.5 RL IR1	12.0 LDE r2, Ir1	18.0 LDEI Ir2, Ir1												6.1 EI
	A	10.5 INCW RR1	10.5 INCW IR1	6.5 CP r1, r2	6.5 CP r1, Ir2	10.5 CP R2, R1	10.5 CP IR2, R1	10.5 CP R1, IM	10.5 CP IR1, IM								14.0 RET
	B	6.5 CLR R1	6.5 CLR IR1	6.5 XOR r1, r2	6.5 XOR r1, Ir2	10.5 XOR R2, R1	10.5 XOR IR2, R1	10.5 XOR R1, IM	10.5 XOR IR1, IM								16.0 IRET
	C	6.5 RRC R1	6.5 RRC IR1	12.0 LDC r1, Ir2	18.0 LDCI Ir1, Ir2				10.5 LD r1, Ir2								6.5 RCF
	D	6.5 SRA R1	6.5 SRA IR1	12.0 LDC r1, Ir2	18.0 LDCI Ir1, Ir2	20.0 CALL* IRR1		20.0 CALL DA	10.5 LD r2, Ir1								6.5 SCF
	E	6.5 RR R1	6.5 RR IR1		6.5 LD r1, Ir2	10.5 LD R2, R1	10.5 LD IR2, R1	10.5 LD R1, IM	10.5 LD IR1, IM								6.5 CCF
	F	8.5 SWAP R1	8.5 SWAP IR1		6.5 LD Ir1, r2	10.5 LD R2, R1											6.0 NOP



Legend:

R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

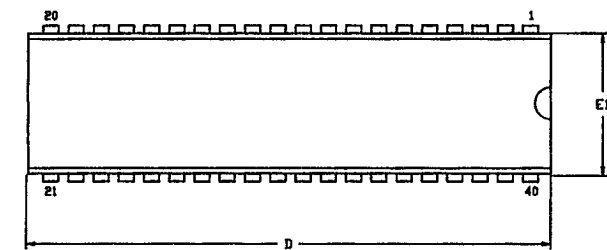
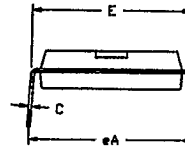
Sequence:

Opcode, First Operand,
Second Operand

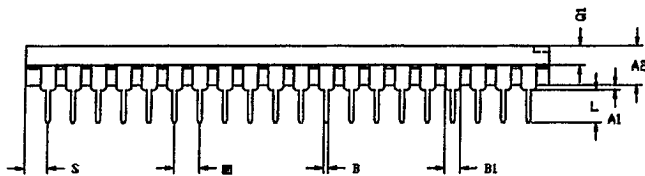
Note: Blanks are reserved.

*2-byte instruction appears as
a 3-byte instruction

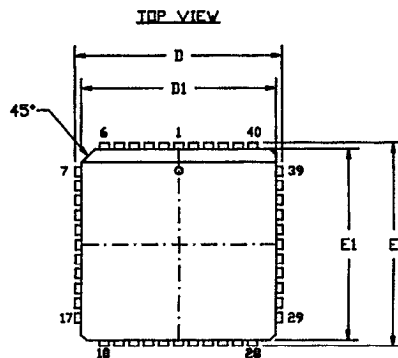
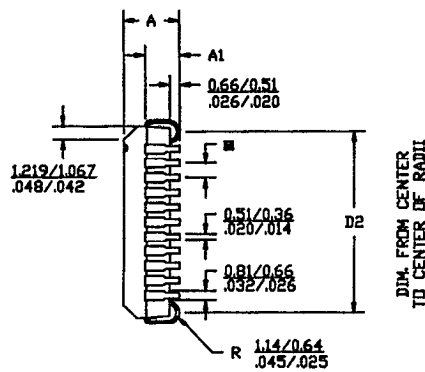
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
■	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090



40-Pin DIP Package Diagram

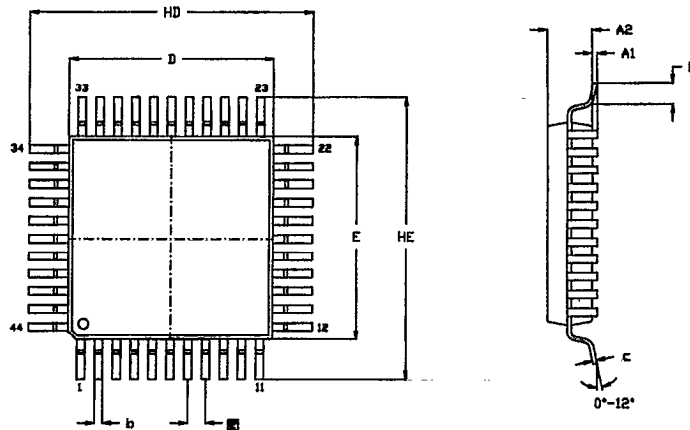


- NOTES:
1. CONTROLLING DIMENSIONS : INCH
 2. LEADS ARE COPLANAR WITHIN .004 IN.
 3. DIMENSION : $\frac{\text{MM}}{\text{INCH}}$

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.67	2.92	.105	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
■	1.27 TYP		.050 TYP	

44-Pin PLCC Package Diagram

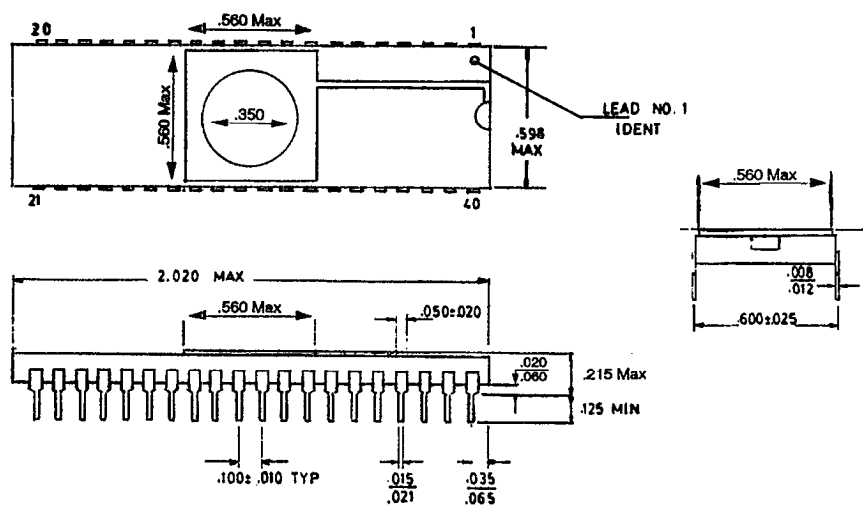
PACKAGE INFORMATION (Continued)



NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 mm
.004"

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.30	.539	.563
D	9.90	10.10	.390	.398
HE	13.70	14.30	.539	.563
E	9.90	10.10	.390	.398
□	0.80 TYP		.031 TYP	
L	0.60	1.20	.024	.047

44-Pin QFP Package Diagram



40-Pin Cerdip Package Diagram

ORDERING INFORMATION

Z86E40

12 MHz

40-Pin DIP

Z86E4012PSC

40-Pin PLCC

Z86E4012VSC

44-Pin QFP

Z86E4012FSC

40-Pin Cerdip

Z86E4012KSE

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Codes

Package

P = Plastic DIP

V = Plastic Chip Carrier

k = Cerdip Window

Longer Lead Time

F = Plastic Quad Flat Pack

Speed

12 = 12 MHz

Temperature

S = 0°C to +70°C

Environmental

C = Plastic Standard

E = Hermetic Standard

Example:

Z 86E40 12 P S C is an 86E40 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow

